THIN FILM ENCAPSULATION OF RADIO FREQUENCY (RF) MICROELECTROMECHANICAL SYSTEMS (MEMS) SWITCHES

THESIS

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Eric Marsh

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Abstract

Microelectromechanical systems (MEMS) radio frequency (RF) switches have been shown to have excellent electrical performance over a wide range of frequencies. However, cost-effective packaging techniques for MEMS switches do not currently exist. This thesis involves the design of RF-optimized encapsulations consisting of dielectric and metal layers, and the creation of a novel thin film encapsulation process to fabricate the encapsulations. The RF performance of several encapsulation designs are evaluated with an analytical model, full wave electromagnetic simulation, and laboratory testing. Performance degradation due to parasitic and reflection losses due to the package is considered, and RF feed-throughs of the transmission line into and out of the package are designed and assessed.

Ten different encapsulation designs were created and their RF performance was characterized in terms of insertion loss, return loss, and isolation. A switch without an encapsulation and a switch with a dielectric encapsulation were fabricated and tested by the Air Force Research Laboratory (AFRL), and the test data was used to verify the data from analytical modeling and electromagnetic simulation performed in this work. All results were used to design an optimized encapsulation. An RF MEMS switch with this encapsulation was shown to have an overall insertion loss of less than -0.15 dB at 20 GHz compared to an unencapsulated switch insertion loss of about -0.1 dB. The isolation of the switch was slightly improved with the encapsulation.

The fabrication process proposed to manufacture these encapsulations uses a low temperature solder as the metal encapsulation layer. As the final step in the fabrication, the solder is brought to melting temperature and reflowed over the etch holes to form a hermetic encapsulation. Analysis was performed to determine the necessary dimensions of the solder thickness and the etch hole width in order to guarantee that the hole will close when the solder is reflowed. The results found that for a square etch hole with a width of 5 μm, the minimum solder layer thickness to guarantee hole closure is 5.17 μm.

THIN FILM ENCAPSULATION OF RADIO FREQUENCY (RF) MICROELECTROMECHANICAL SYSTEMS (MEMS) SWITCHES

1. Introduction

The field of microelectromechanical systems (MEMS) is rapidly growing, and research is ongoing in many different MEMS devices for a wide range of applications. One such device is the radio frequency (RF) MEMS switch. RF MEMS switches are used for the switching of RF electrical signals, and have been shown to have excellent electrical performance at a wide range of frequencies (DC to greater than 120 GHz) [1]. Although excellent devices have been demonstrated in research, many obstacles still remain before MEMS switches will be viable for widespread use. Packaging remains as one of the main areas to be addressed. Only after cost-effective packaging methods are developed will RF MEMS switches be able to transition from research and high-end defense applications to commercially viable products, as is the case with semiconductor-based RF switches today.

1.1. Background

New technologies are always being explored with the goal of increasing the performance of defense and consumer products. One field that has been growing very quickly in recent years is wireless systems. Wireless systems all employ radio frequency

(RF) or microwave electronics in order to transmit and receive signals. One of the components in most of these RF systems that has a direct impact on the overall performance of the system is the RF switch. For example, many wireless devices are battery powered, and battery life is a performance metric for the system. A more efficient RF switch results in a longer battery life in a battery powered system. Other performance metrics of RF switches also directly result in higher performance for the systems in which they are used. This motivation has lead consumer companies to research RF switches for use in systems such as mobile phones and instrumentation systems. Similarly, some defense applications that will benefit from better RF switches are radars, communication systems, and satellite systems.

Current state-of-the-art RF switches are based on MESFETs (Metal-Semiconductor Field Effect Transistor) and PIN diodes. RF MEMS switches have been shown to have superior electrical performance to semiconductor-based switches, but are not yet cost-effective for use in anything but high-end defense and research applications. One of the major challenges to date for producing RF MEMS switches is how to package them. Because MEMS devices are mechanical in nature, they require a stable environment for consistent and reliable operation. Ideally the packaging for these switches will incorporate a hermetic (air tight) seal. The only economically feasible way to do this is wafer-level packaging, where every device on a wafer is sealed at once in some type of encapsulation.

The Air Force Research Laboratory (AFRL) has demonstrated a novel packaging process for RF MEMS switches based on the same thin film processes that were used to fabricate the RF MEMS switches they also developed. Their technique involves deposit-

ing a sacrificial layer over the MEMS switch, then depositing a structural encapsulation layer of a dielectric such as silicon nitride over the sacrificial layer. The sacrificial layers are then removed, leaving an encapsulated device.

The work in this thesis will differ from existing packaging research in several ways. First, it will use low temperature thin film fabrication techniques that are compatible with RF MEMS switches. Second, the analysis on the designs will be used to create an optimized encapsulation in terms of its RF performance. Third, the encapsulations will incorporate a metal layer of a low melting temperature solder as part of the encapsulation, which is reflowed in the last step of the encapsulation to seal the etch holes.

1.2. Problem Statement

High performance RF switches are in demand for many defense and consumer applications. RF switches based on MEMS technology have been shown to have very high performance, but packaging them in a cost-effective manner is difficult. Packaging for RF MEMS switches must provide protection from physical damage and contamination, and must provide the switch with a hermetic encapsulation for reliable, long-term operation. Also, the packaging must have little or no detrimental effect on the RF performance of the switch. Due to these special requirements for RF MEMS switch packaging, cost-effective methods for this packaging do not currently exist. The specific problem for this research is to design an encapsulation for RF MEMS switches that is optimized in its RF performance, based on modeling and experimentation. These encapsulations will incorporate a metal layer, and will be able to be fabricated with standard thin film techniques. A fabrication process than can be used to fabricate the encapsulations will also be created.

1.3. Proposed Solution

An optimized RF encapsulation will be designed based on results from analytical modeling and electromagnetic simulation of preliminary design. AFRL has fabricated and tested RF MEMS switches with dielectric encapsulations that were fabricated using thin film methods. The work in this thesis will build on the AFRL research by incorporating a metal layer in the encapsulation. The geometry of the encapsulations and the materials used for the encapsulations will be considered in the designs. The test data from AFRL's unencapsulated RF MEMS switch and one with a dielectric encapsulation will be used to verify the analytical model and electromagnetic simulation. The model and simulation are then used to evaluate other designs and to create an optimized design. RF feed-throughs of the transmission line into and out of the encapsulation will also be designed and evaluated to increase the overall performance of the encapsulated switch. Next, an analysis of metal reflow over etch holes will also be performed to determine the proper geometry for the metal layer to seal the etch holes shut when the metal is brought to melting temperature. Finally, a fabrication process based on thin film techniques will be devised that can be used to fabricate the encapsulations.

1.4. Novel Contributions of This Work

The novel contributions of this work are summarized briefly below:

- Design of MEMS encapsulations that consist of a dielectric layer and a metal layer
- Development of an analytical model for assessing the performance of RF MEMS switch encapsulations that consist of dielectric and metal layers
- Development of a novel thin film fabrication process for fabricating the proposed MEMS encapsulations

- Creation of an optimized RF MEMS package through the use of analytical modeling and electromagnetic simulation
- The proposal of using sputtered silicon nitride as a dielectric encapsulation layer
- The proposal of using solder reflow to seal the etch holes in a MEMS encapsulation
- Analysis, based on fluid surface energy, of the required thickness and width of a square etch hole to ensure that the hole will seal shut when the solder is reflowed

1.5. Document Road Map

A thorough explanation of conventional RF switches, MEMS, RF MEMS switches, RF MEMS packaging, and RF performance measures are provided in Chapter 2. Chapter 3 describes in detail the encapsulation designs that were created and evaluated as part of this work, including their geometries and material parameters. Chapter 4 provides the development of the analytical models used to describe the performance of the encapsulations over each RF MEMS switch, and the development of an RF feedthrough of the transmission line into the encapsulation. It also describes the methodology for modeling metal reflow over an etch hole. In Chapter 5 the procedures and details of the full-wave electromagnetic simulation that was used to assess the performance of the encapsulation designs are described. In Chapter 6 the instrumentation set up and measurement procedures for collecting test data are given. In Chapter 7, all results from modeling, simulation, and testing are compared and discussed, including the results from metal reflow modeling. Based on the results, an optimized encapsulation design is given in Chapter 8, along with a detailed explanation of the thin film fabrication process that is proposed to fabricate the encapsulations. Chapter 9 summarizes all work that was com-

pleted and gives direction for areas of follow-on research. Appendix A gives the details from the software package that was used to perform finite element modeling on the structures to determine accurate values for capacitance. Appendix B gives the computer code that was written to calculate the model parameters for the analytical model. Appendix C gives some coplanar waveguide theory and design calculations that were used to calculate the RF feed-through, along with the computer code that was written to make the calculations. Appendix D gives the input file to the metal reflow modeling software that was used in this research. Appendix E gives the code that was written to create the data plots that are shown in Chapter 7 of this thesis.

1.6. References

[1] Rebeiz, G. M., *RF MEMS Theory Design, and Technology*, Hoboken, NJ: Wiley-Interscience, 2003.

2. Background

Switches are essential components in most electrical systems. The concept of a switch is quite simple: it makes or breaks a circuit. A great deal of research is currently being done on how to design and produce efficient switch circuits for high frequencies. At radio frequencies (RF) and microwave frequencies, the design of any electrical circuit becomes more difficult because the corresponding wavelengths for these frequencies are on the order of the feature sizes of the circuits. When this occurs, the phase of the voltage or current on a circuit is different at different points in the circuit, and standard lumped element theory does not accurately model the circuit. Electromagnetic theory based on Maxwell's Equations must be used to model high frequency circuits and devices such as switches.

Many different types of switches exist today for high frequency applications. Electromechanical switches, such as coaxial switches, offer outstanding electrical performance, but are relatively large, heavy, and expensive. RF switches based on semiconductor technologies, the PIN diode and MESFET, offer very good electrical performance and small size, and consequently are what is used predominantly in RF applications today. Recently, much attention has been given to high frequency switches based on MEMS technologies. MEMS switches offer superior electrical performance over semiconductor-based switches in many areas, and these improvements contribute directly to increased performance in the systems in which they are used.

This section will describe the motivation for RF MEMS switches by first describing the predominant RF switches today, those based on semiconductor technology, and their shortcomings. Next MEMS are introduced as a new technology for RF switches that

can improve on the performance of semiconductor-based RF switches. The field of MEMS is described and a typical MEMS fabrication process is explained. Next, MEMS switch operation, advantages, and disadvantages are described. This leads to the identification of one current challenge of RF MEMS switches: packaging. Several different MEMS packaging technologies are surveyed and explained, along with their advantages or shortcomings for packaging RF MEMS switches. Next, a packaging process that is under research at the Air Force Research Laboratory (AFRL) is discussed. This process is the baseline for further research described in this thesis. Finally, RF figures-of-merit for RF MEMS switch performance characterization are defined. These figures-of-merit will be used throughout this report to describe and compare RF MEMS switch and encapsulation performance. Also included is a survey of research on design and performance characterization RF MEMS switch packaging.

2.1. Semiconductor-based RF Switches

2.1.1. PIN Diode Switches

A PIN diode's name indicates its makeup; Figure 2.1 shows in a simplified drawing of the semiconductor regoins that it consists of a P-type semiconductor and an N-type semiconductor that sandwich an intrinsic region. It is specified by cross section area A, and intrinsic region width W. PIN diodes operate similarly to p-n junction diodes, but the addition of the intrinsic region results in very high values for the breakdown voltage in reverse bias. When used as a switch, the devices are biased as to operate in a binary scheme: they are reverse biased to attain the highest resistance possible from the device for an open circuit, and they are forward biased to attain the lowest resistance possible for a closed circuit [1].

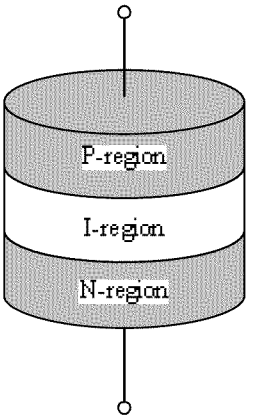


Figure 2.1. Simplified drawing of the structure of a PIN diode showing the electrical contacts and the three semiconductor regions.

The forward bias case occurs when a positive voltage is applied across the diode (from P to N). In this case, holes from the p-region and electrons from the N-region are injected into the intrinsic region. These charges do not recombine immediately, so a net charge always exists in the intrinsic region under forward bias. This net charge causes the resistivity of the region to decrease. When the device is fully forward biased, the resistivity is very small, but finite. This results in a finite loss for these devices when operated in series with the RF signal, which is usually the case when used in RF switch circuits.

The negative bias case occurs when a negative voltage is applied across the diode (also from P to N). In reverse bias, the voltage causes any charge carriers in the I-region to move out of the I-region, fully depleting it, and a very high resistance across the diode results. At high frequencies in reverse bias, the device's performance is best characterized by the capacitance across the N- and P-regions. This capacitance determines the device's isolation—a measure of how well the device prevents current from 'leaking' through in the 'off' state. This physical separation of the P- and N-regions makes the PIN diode more suited for RF applications than a standard p-n diode.

Due to its ability to have a low resistance in forward bias, and very high resistance and large capacitance in the reverse biased state, the PIN diode works well as a switch. One of the main disadvantages of PIN diode based switch circuits is that they must always have a bias current applied to them. This results in continuous power consumption which makes them unsuitable for many applications, especially those that rely on batteries for power.

2.1.2. MESFET Switches

The MESFET (Metal Semiconductor Field Effect Transistor) is another common active device for RF and microwave frequencies [1]. GaAs (Gallium Arsenide) is frequently used as the substrate to maximize the performance of the device for high frequencies. Electron mobility is 5-10 times higher in GaAs than it is in Si, which results in higher speeds of operation for GaAs devices than for Si devices. The higher electron mobility of GaAs compared to Si also results in a lower resistance in the channel for transistors of similar area.

GaAs MESFETs, like silicon MOSFETs can be viewed as voltage controlled resistors. By controlling the gate bias, the channel can be switched between a low impedance state (closed circuit) and a high impedance state (open) circuit. The standard MESFET is a depletion-type device. Figure 2.2 shows a drawing of a MESFET, with the different semiconductor regions identified. At zero bias, the active region conducts current freely since no depletion region is introduced into the active region below the gate. Because current flows in the unbiased state, it is referred to as 'normally on.' As negative voltage is applied to the gate, a depletion region is formed under the gate. Current cannot flow through the depletion region, so as the negative bias voltage is increased (more

negative) the channel made narrower, and the resistance of the channel is increased. As gate voltage is increased, the conducting channel is eventually is pinched off, preventing current from flowing through the channel.

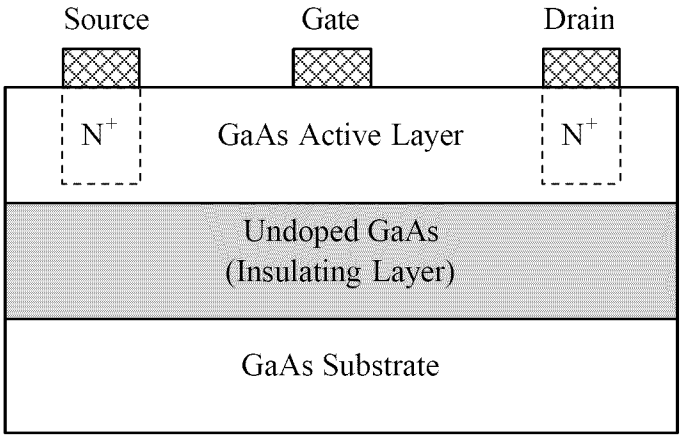


Figure 2.2. Simplified drawing of the material structure of a MESFET.

This ability to bias the MESFET to have an open or closed channel is exploited to use the device as a switch. MESFET-based switches have higher speeds that PIN diode switches, but suffer from higher insertion loss due to the finite resistance of the semiconducting channel. Again, one example of how lossy switches affect RF systems is decreased battery life of battery-powered systems.

2.2. MEMS

Effective RF switches can also be fabricated with MEMS technology. This section describes what is meant by "MEMS," and how MEMS are fabricated.

2.2.1. What are MEMS?

Microelectromechanical Systems (MEMS) refers to the field of fabricating systems and devices with dimensions on the order of 1 micron (or 1 μm). Although the name "MEMS" implies the systems employ both mechanical and electrical aspects, many

MEMS systems have neither. The name MEMS is used as more of a general term for micron-scale systems and devices and the discipline around designing, fabricating, and understanding them. The discipline of MEMS involves knowledge of the intended application, material properties, microfabrication, and scaling laws [2]. In order to appreciate what MEMS are, an understanding is needed of how they are fabricated, which is discussed in the next section.

2.2.2. MEMS Fabrication

The three most common technologies for fabricating MEMS today are bulk micromachining, surface micromachining, and micromolding. In the area of RF MEMS switches, surface micromachining is used almost exclusively for fabrication, so it will be covered in greater detail here, while bulk micromachining and micromolding will only be briefly described.

Micromolding is a technology that was developed in Germany. The original process that was developed and used today is called LIGA. LIGA is an acronym for the German words "LIthographie, Galvanoformung, Abformung," meaning lithography, electroplating, and molding. LIGA employs a thick layer (micrometers to millimeters) of x-ray resist that is exposed through a mask to high power x-rays. The subsequent development of this resist results in a high aspect ratio resist structure that can subsequently be used as a sacrificial mold to create microstructures by filling it with metal through metal deposition processes. The resulting metal microstructure may be the end product itself, or it may be used to produce additional, identical micromolds. These micromolds can be made of cheap, easy to use materials such as plastic, which makes mold creation and filling cheaper and easier than with resist. These resulting micromolds can then be used to

mass produce metallic structures through metal deposition. LIGA is capable of yielding extremely high aspect ratio (>100:1) metallic structures of thicknesses up to the millimeter range [3]. One of the reasons this method is not more widespread is because it requires a high precision x-ray source known as a synchrotron, a highly specialized and very expensive piece of equipment.

Bulk micromachining is a subtractive process that refers to the selective etching of the substrate to sculpt desired geometries from it. This etching is typically performed with wet chemical etchants. Control over the geometry of the etching is enabled by the use of anisotropic etchants that etch different crystal planes of crystalline substrate materials (usually silicon) at different rates. This property is exploited to create high aspect ratio structures and suspended mechanical parts. An example is shown in Figure 2.3. In the figure, silicon has been etched by bulk micromachining. The piece of silicon shown was assumed to have had a square etch mask on its surface, and was exposed to a anisotropic etchant. The top view in Figure 2.3(a) shows the square area of the substrate that was allowed to be etched. Figure 2.3(b) shows a side cross-section of the pit that was etched into the substrate. Control over the depth of the pit is achieved through timing of the etch. A longer etch would continue to deepen the pit until it etched all the way through the substrate. This procedure is used to create micronozzles for fluid flow. Viewed from the bottom side of the wafer, the pit shown in Figure 2.3(b) is a thin membrane where the substrate has been etched away underneath it. Membranes such as this are the basis for many MEMS sensor designs. Standard integrated circuit electronics can then be fabricated onto the wafer and membrane to create an integrated sensor.

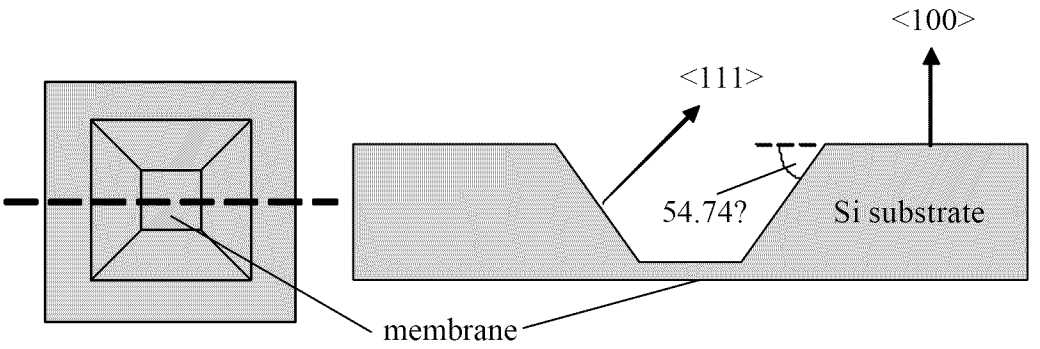


Figure 2.3. (a) Top view and (b) side cut-away drawings of a v-shaped pit created by bulk micromachining of silicon using anisotropic etching.

Surface micromachining is an additive process that is an extension of well-established integrated circuit (IC) fabrication technologies such as photolithography, thin film growth and deposition, and dry etching. Surface micromachining involves the deposition and patterning of two types of layers: structural and sacrificial. The structural layers make up the mechanical parts and electrical conductors, and are typically made of polysilicon, gold, aluminum, titanium, platinum, nickel, silicon carbide, silicon dioxide, silicon nitride, or other similar materials. The material for the structural layer is chosen based on its material properties. Based on the application for the device, it may be desirable to have favorable mechanical or electrical properties. The sacrificial layers are used in the process to create suspended parts, gaps, and 3-dimensional structures. In MEMS fabrication, the sacrificial layer is etched away, or released, as the last step in surface micromachining to create movable or freestanding microstructures. The sacrificial layer is typically made of resist, phosphophosilicate glass (PSG), silicon dioxide, photoresist, or other easily patterned and etched materials.

Surface micromachining is the fabrication process used by AFRL to create their RF MEMS switches. In their process, gold is used as the structural material for the deformable suspended beam and for the electrical conductors. Polymethylglutarimide (PMGI) is used as the sacrificial layer for the suspended beam. PMGI is polymer-based electron beam (e-beam) resist that has a higher reflow temperature than optical resist, is not affected by UV light, can be used in conjunction with optical resist without chemical interactions, and is not affected by optical resist developers or strippers. Silicon nitride or aluminum oxide (alumina) is used as the RF dielectric, whose function will be described in Section 2.3.2.

The fabrication process is shown in Figure 2.4. The process starts with a dielectric substrate, such as alumina, quartz, or sapphire. First, 300 nm of gold is deposited by evaporation and patterned with lift-off using 1813 or 1805 optical resist to create the coplanar waveguide (CPW) lines as shown in Figure 2.4(a). Next, Figure 2.4(b) shows that 200-250 nm of aluminum oxide is deposited and patterned with photolithography over the center conductor of the CPW at the point where the bridge will contact it when actuated. This layer is the RF dielectric, whose function is described in Section 2.3.2. Figure 2.4(c) shows the next step, where 3 μm of PMGI is spun over the wafer, and patterned with photolithography to create the sacrificial layer between the CPW and the bridge that will be formed over it. After patterning, the PMGI is reflowed at 250°C to create rounded sidewalls on the sacrificial layer. These rounded sidewalls are necessary because evaporation is again used to deposit the gold suspended beam layer, and evaporation provides poor step coverage because it is a non-conformal deposition method [4]. Figure 2.4(d) shows the next step, where a 600-700 nm layer of gold is deposited by

evaporation and patterned with lift-off using optical resist. This layer is the suspended bridge, and it is anchored at each end to the ground planes of the CPW and suspended by the sacrificial layer between the anchors. The final step is a bath in PMGI stripper to remove the sacrificial layer and release the bridge as a suspended, movable structure as shown in Figure 2.4(e). Immediately following the release the switch is dried using a supercritical CO_2 drying process to avoid stiction. A scanning electron microscope (SEM) image of a switch fabricated with this process is shown in Figure 2.5, with all dimensions annotated on the image. A cut-away drawing of the switch is also shown so the vertical dimensions (layer thicknesses and gap widths) can be shown.

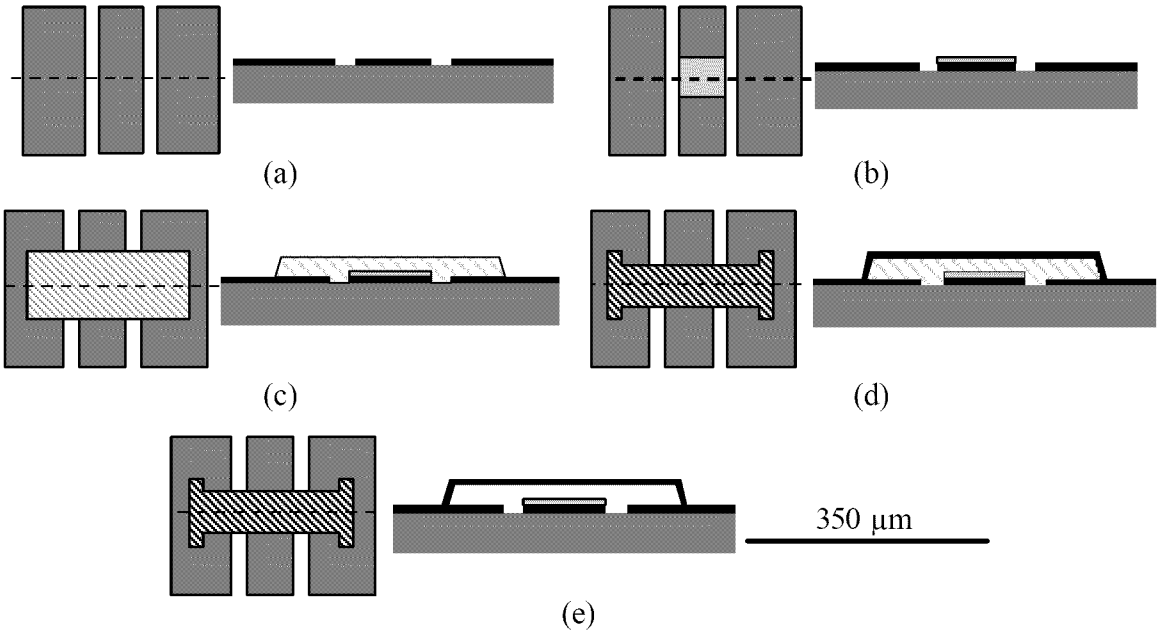


Figure 2.4. Step-by-step top view and side cut-away drawings of the fabrication process for AFRL capacitive switches: (a) the gold CPW lines are deposited and patterned; (b) the RF dielectric layer is deposited and patterned; (c) the sacrificial layer for the suspended beam is deposited, patterned, and reflowed; (d) the gold suspended beam is deposited and patterned; (e) the sacrificial layer is released. Note that the vertical dimension is greatly exaggerated for clarity.

The additional steps that AFRL is currently adding to the process to create encapsulations for each switch will be described in Section 2.7.3. Now that MEMS and their fabrication have been described, in the next section the advantages of applying MEMS technology toward RF switches will be explained.

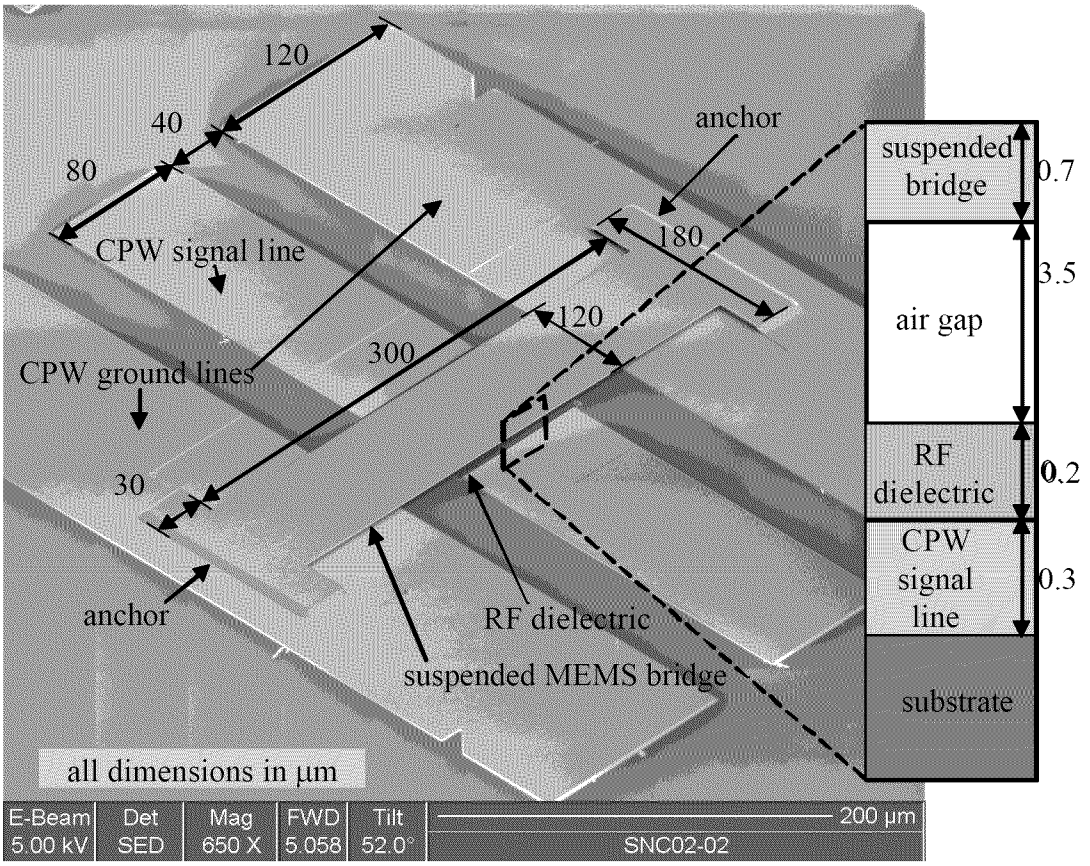


Figure 2.5. Annotated SEM image of the AFRL capacitive switch that was tested and packaged, including a cut-away drawing of the center of the switch to show vertical dimensions [5].

2.3. RF MEMS Switches

Clearly there is much motivation to have efficient RF switches. A great deal of research has been done and is ongoing in creating RF switches using MEMS technology because of several demonstrated advantages of RF MEMS switches over existing tech-

nologies. However, several disadvantages or challenges exist for RF MEMS switches that are the focus of much of the ongoing research on the devices.

2.3.1. Advantages and Disadvantages

The following advantages are inherent to MEMS switches, and are in most cases improvements over the performance of MESFET and PIN diode based switches: [2]:

Low Power Consumption: electrostatically actuated MEMS switches often require high actuation voltages (20-80 V), but need almost no current, so the resulting power dissipated in driving the switch is very small.

High Isolation: MEMS switches are fabricated with an air gap when the switch is open. This air gap results in high values for isolation over a broad band of frequencies.

Low Insertion Loss: This figure of merit is often the most critical in high performance systems, and semiconductor-based switches do not excel in insertion loss. MEMS switches have shown insertion losses on the order of -0.1 dB up to 40 GHz.

Low Intermodulation Products: MEMS switches are very linear, so they have very low intermodulation products. Semiconductor-based switches have much poorer intermodulation performance since semiconductors are inherently nonlinear devices.

RF MEMS switches also have several disadvantages and challenges. Some of them are inherent to the devices, but others are challenges that have not been solved with research at this time since RF MEMS switches are a relatively new technology. The major disadvantages and challenges are:

Slow Switching Speed: Because MEMS are mechanical devices, they are limited in how fast they can effectively actuate. Semiconductor switches are very fast because they have no moving parts, and the limiting factor is the speed of the electrons within the

device. In some communications and radar applications, MEMS switches do not meet switching speed requirements.

Low Power Handling: Most MEMS switches cannot handle more than 50 mW, and even the best examples of power handling in research can only handle about 500 mW of power with any reliability.

High Actuation Voltage: Although they consume very little power, they often re-qure high voltages for actuation, which will increase the complexity of the drive circuitry, and therefore the cost of using the switch in a system.

Reliability: Long term reliability that is required for many applications (20-200 billion cycles) has not been achieved or proven in most MEMS switches. In addition, the mechanisms that cause premature switch failure are not well understood.

Packaging: Because they have delicate microstructures, MEMS switches require special handling and packaging, and cost-effective methods for packaging have not been demonstrated to date. This topic will be discussed in more detail in Sections 2.4-2.8.

2.3.2. Design and Operation

A variety of physical mechanisms exist for actuating MEMS structures: electrostatic, electromagnetic, electrothermal, residual stress, and shape memory. Electrostatic actuation is regarded to be the most feasible mechanism to use for actuating MEMS switches due to low power consumption, simplicity in design and fabrication, and favorable scaling of electrostatic forces to the micro-scale. Electrostatic switches exploit the electrostatic attraction of oppositely charged objects. Although electrostatic force in the macroscopic world is negligible, at the microscopic scale (feature sizes on the order of one micron, or 10^{-6} meters), the forces scale favorably and can be used for actuation. The

AFRL RF MEMS switch designs are electrostatically actuated, and are what will be considered in this research exclusively.

Most electrostatically actuated MEMS switch designs are either a suspended cantilever (diving board) design as shown in Figure 2.6(a), or a bridge structure as shown in Figure 2.6(b). Both of these structures exploit electrostatic force by applying a voltage across the suspended beam and the electrode on the substrate directly below it. When enough actuation voltage has been applied to the lower electrode, the beam collapses down onto the electrode. A drawing of how this would look for a fixed-fixed beam electrostatic actuator is shown in Figure 2.7. The amount of voltage that is required to do this is called the pull-down voltage, pull-in voltage, snap-down voltage, or the snap-through voltage. The pull-in voltage is important in a MEMS switch because it is the minimum voltage required to actuate the switch. Note that although a voltage is necessary to actuate the switch, very little power is consumed in the process because of low current. This is achieved by designing the electrical connection lines to the electrodes to be high resistance lines.

The operation of this switch is relatively simple, and this simplicity is an inherent advantage of electrostatically actuated switches. In the "up" state (or "off" state), the beam is separated from the RF signal line by the thickness of the RF dielectric and by the air gap. This distance is relatively large, so the capacitance between the RF signal line and the bridge is very small, and the resulting electromagnetic coupling between them is also small. This negligible coupling in the "up" state results in very low insertion loss for this switch. To actuate the switch, a bias (actuation) voltage is applied to the RF signal line, while the outer conductors of the CPW are held at zero potential. At pull-in, the

beam collapses downward and rests on the RF dielectric. Because the gap between the beam and the RF signal line is very small (only the thickness of the RF dielectric), the resulting capacitance between the two conductors is much larger than before (than the non-actuated state), and the signal electromagnetically couples very efficiently through the RF dielectric layer to the collapsed bridge. This results in the RF signal being switched off by being connected to ground. RF MEMS switches that use electromagnetic coupling as just described instead of ohmic contact are known as capacitive switches. These switches are designed only for high frequency operation, and do not work at all at DC. The avoidance of any metal-to-metal contact in capacitive switches allows them to avoid the long-term reliability issues that plague metal contact switches.

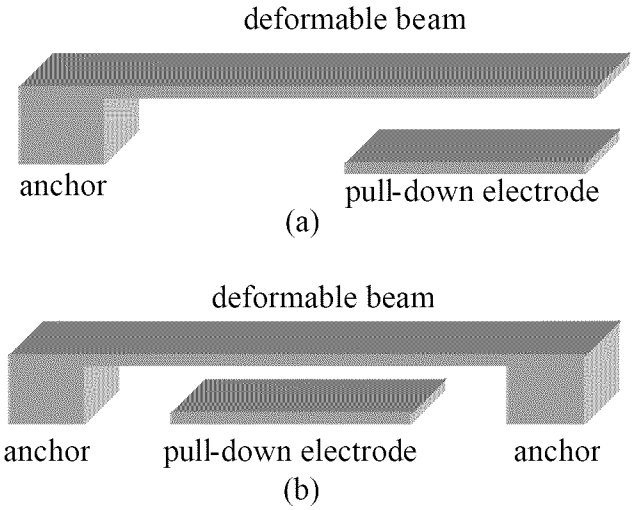
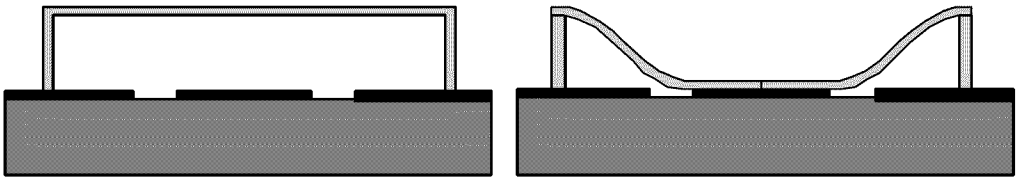


Figure 2.6. Simplified drawings of the two main types of electrostatically actuated MEMS switches; (a) cantilever switch; (b) fixed-fixed beam switch, showing the anchors, deformable beams, and pull-down electrodes.

One reason the AFRL switches are based on CPW is the simplicity of testing CPW-based devices on-wafer. However, these designs can easily be modified to operate on different transmission lines such as microstrip lines.



(a) (b)

Figure 2.7. Side view drawings of a fixed-fixed beam MEMS switch in operation: (a) switch in the unactuated (up) state; (b) switch in the actuated (down) state, where the beam is deformed down to the lower electrode. Note: the vertical dimension is exaggerated for clarity.

While designing efficient RF switches is challenging, one additional challenge is packaging the switches in a cost-effective manner that still allows the switches to operate at optimum performance. These challenges and some packaging approaches are covered in the following sections.

2.4. RF MEMS Switch Packaging

While development and maturity of MEMS switches has been rapid over the last several years, the development of suitable packaging technologies has not kept pace. Currently it is relatively inexpensive on a per-unit basis to batch produce MEMS switches. However, packaging these switches with existing technologies pushes the per-unit cost into levels that make them too expensive for most applications. Because of this, research is ongoing on several different approaches to cost-effective packaging of RF MEMS switches. This section will discuss what is meant by packaging, why MEMS switches must be packaged, special requirements for MEMS switch packaging, and current approaches to the problem.

The discipline of packaging is very broad. For microelectronics, packaging involves connection of power and signals to a chip-level die, heat dissipation, and protec-

tion from the environment. The package must meet these requirements at the same time as meeting performance requirements for the packaged device. As defined in the packaging text by Pecht, packaging is done on five levels, each with its own requirements [6]:

- Zero-level packaging – The die itself that includes interconnections between different components on the die.
- Level 1 packaging – The die is put in a larger package made of metal, ceramic, plastic, or other materials, and the die is wired to the package.
- Level 2 packaging – Multiple chips are packaged together into one module. This level of packaging is sometimes not used or needed.
- Level 3 packaging – Several Level 1 and/or Level 2 packages, along with discrete circuit components, are integrated into a circuit board, often with interconnections printed on it.
- Level 4 packaging – Several circuit boards are integrated together, along with associated power circuits, cooling, and an enclosure, to create a fully packaged working product.

In general, MEMS components can't be packaged with the same standard technologies that are used for microelectronics packaging, especially for Level 0 and Level 1 packaging. Because MEMS switches have fragile microstructures, they must be handled more carefully in the packaging process. In addition, the structures may be destroyed if they are contaminated by dirt or debris during the packaging. Because of these facts, many believe each MEMS switch on the wafer must be packaged at Level 0 before the wafer is subdiced. These zero level packages will encapsulate each MEMS switch on the wafer and protect them from the later stages of packaging. Furthermore, the only cost-effective way to encapsulate each device on the wafer is to encapsulate all of them at once. This is known as wafer-level encapsulation, or wafer-level packaging. Once each device is packaged, the wafer may be subdiced and each die handled and packaged with

standard technologies. The encapsulated dies would not require special handling, which would save money over attempting to package MEMS switches with conventional packaging technologies without a zero-level encapsulation.

Some other special requirements exist for MEMS switch packaging. First, MEMS switches must be packaged in sealed encapsulations because they are very sensitive to humidity, dirt, or contaminants. Ideally the cavity will be filled with a dry, inert gas, and the package will be hermetically (air tight) sealed. Humidity and contamination must be kept out of the encapsulation because they may cause a switch to stick in the "down" position, a phenomenon known as stiction. Once a MEMS switch is stuck down due to stiction, it is useless, so it is critical that this condition be avoided.

It is possible to package MEMS switches using conventional packaging techniques. The process and its shortcomings are explained in the next section.

2.5. Conventional Packaging of RF MEMS Switches

Packaging of MEMS using conventional (IC) methods involves subdicing the MEMS wafer and attaching each die to a ceramic chip carrier with a low-temperature epoxy. Figure 2.8 shows a drawing of a MEMS device that is undergoing conventional packaging in a standard chip carrier package. The MEMS devices are then released, so all subsequent steps must be carried out in ways as not to damage or contaminate the device. Next, in a controlled pressure environment, a top cover (usually glass) is placed over the chip carrier and hermetically sealed, as shown in the figure. This sealing requires a local temperature at the sealing ring of 300-600°C, but the MEMS chip does not necessarily reach those temperatures. Again, special handling is required in this process because each die is unprotected during packaging. This special handling, and the inherently serial

packaging process results in a per-unit packaging cost of $30-$50 for a package with two RF ports and several DC ports, suitable for 6-18 GHz applications, according to Rebeiz [2]. These costs make the parts viable only for high-end defense applications. Clearly, to make packaging cost-effective, it is generally understood that packaging needs to occur at the wafer level. That is, the individual devices need to be protected by an encapsulation before the wafer is cut into individual units. Two general approaches exist for wafer level packaging. The first involves aligning an encapsulating wafer over the MEMS device wafer and bonding the wafers together to form encapsulations. The second method employs surface micromachined structural and sacrificial layers to create encapsulations through standard thin film deposition and patterning processes. These approaches, along with published examples of each, are explained in the following sections.

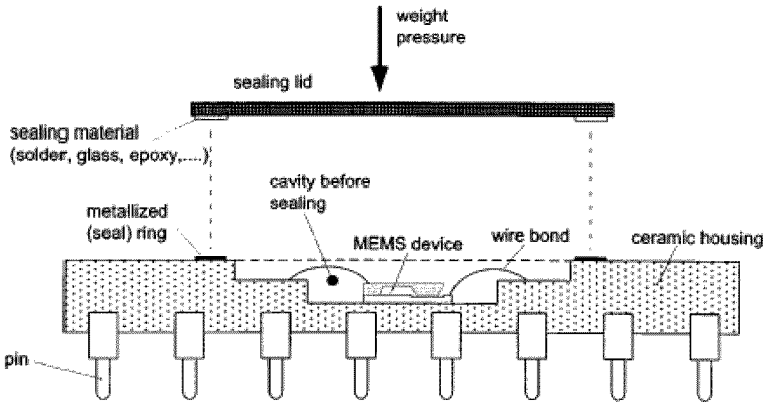


Figure 2.8. Illustration of conventional packaging for MEMS devices using a ceramic package with a sealing lid [7].

2.6. Wafer Bonding

As shown in Figure 2.9, a generic wafer bonding method involves fabricating MEMS devices on one wafer, and fabricating the encapsulations for each MEMS device on another wafer. The two wafers are then aligned and bonded together to create hermeti-

cally sealed encapsulations for each device. Next, the wafer can be subdiced (scribed into individual units) for further packaging. The wafer bonding method has an advantage of producing a zero-level package that is very strong, and can easily withstand standard IC packaging processes such as plastic injection molding. Several technologies for wafer bonding exist, and will be described briefly below.

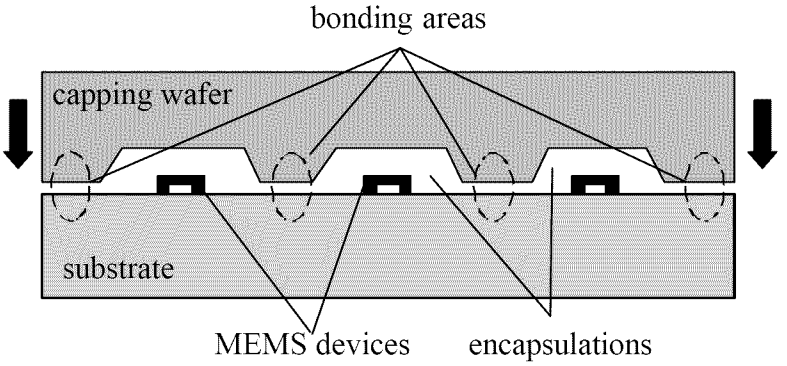


Figure 2.9. Drawing depicting the wafer bonding approach to MEMS encapsulation. The upper wafer has cavities fabricated in it that align over the MEMS devices on the lower wafer. Next, the two wafers are bonded together using various methods. After bonding, the wafer is cut into individual units for further packaging.

2.6.1. Anodic Bonding

Anodic bonding, sometimes also called electrostatic bonding, exploits the fact that glass can be bonded to other materials such as silicon or metals at temperatures below the melting point of glass if it is in the presence of a strong electric field. Figure 2.10 shows a drawing of anodic bonding of glass silicon. In the figure, the glass wafer is attached to a metal cathode and the silicon wafer is attached to a metal chuck. The cathode and chuck are attached to a high voltage source, and the wafers are put in an oven at 300-1000°C. This bonding method can be applied to wafer bonding for MEMS packaging. In a study by Ziaie et al., voltages of 300-2000 V were used at temperatures from 300-450°C [8]. This method results in a mechanically strong hermetic seal and is useful for many MEMS

devices. In fact, experimentation has shown the resulting bond to be stronger than the materials it bonded. However it is not an option for MEMS switches because they typically consist of at least one layer of metal. The temperatures required for anodic bonding would damage or destroy the metal in the switches, rendering them useless. In addition, the bonding of two different materials at a high temperature will result in residual stresses in the wafer due to thermal expansion mismatches in the two wafer materials. Yet another factor that must be accounted for in anodic bonding is the surface roughness of the two surfaces that are being bonded. Surfaces that are too rough may result in a mechanically weak bond that is not hermetically sealed. Anodic bonding can also be used to bond silicon to silicon if a thin layer of glass is deposited between the two wafers at the bonding points.

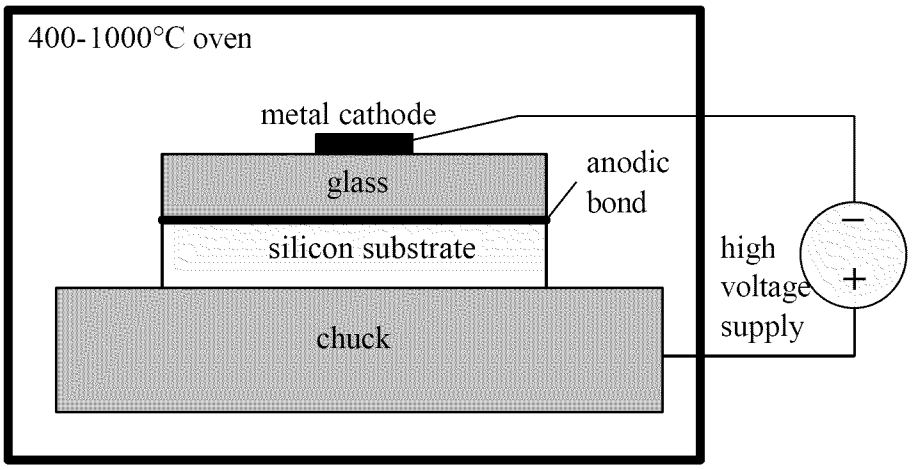


Figure 2.10. Drawing depicting the anodic bonding process for wafer bonding of silicon to glass.

2.6.2. Silicon Fusion Bonding

Silicon can be bonded directly to silicon using fusion bonding. This bonding occurs due to a chemical reaction between the wafers at elevated temperatures. According

to Cheng et al., fusion bonding typically takes place at temperatures above 1000°C [9]. Figure 2.11 gives a drawing of two silicon wafers that are undergoing fusion bonding in an oven at 300-800°C. The result is a hermetically sealed, mechanically strong bond. Thermal mismatch stress is not an issue because the two wafers that are bonded are of the same material. However it is not suitable for MEMS switches because they contain metal parts that would be damaged by high temperatures required in the bonding process. In addition, the hermeticity of the seal is highly dependent on surface roughness, further complicating the process.

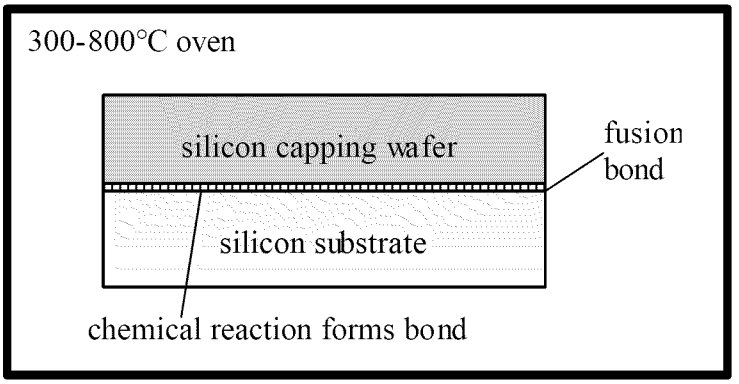


Figure 2.11. Drawing depicting the silicon fusion bonding process for wafer bonding of silicon to silicon.

2.6.3. Eutectic Bonding

At 363° C, gold and silicon diffuse together to form an alloy known as a eutectic mixture. This is the lowest temperature for bonding silicon and gold, even though it is below the melting point of both materials. This mechanism can be used to bond silicon to silicon if a layer of gold exists between them, as described by Cheng et al. [9]. Figure 2.12(a) shows a eutectic bond being formed with silicon and gold in an oven at 363°C. Figure 2.12(b) shows the wafers after the bond has cooled. As in the case of an-

odic and fusion bonding, the high temperature required to reach the eutectic state is too high for RF MEMS switches, so it is not a suitable bonding process for these devices.

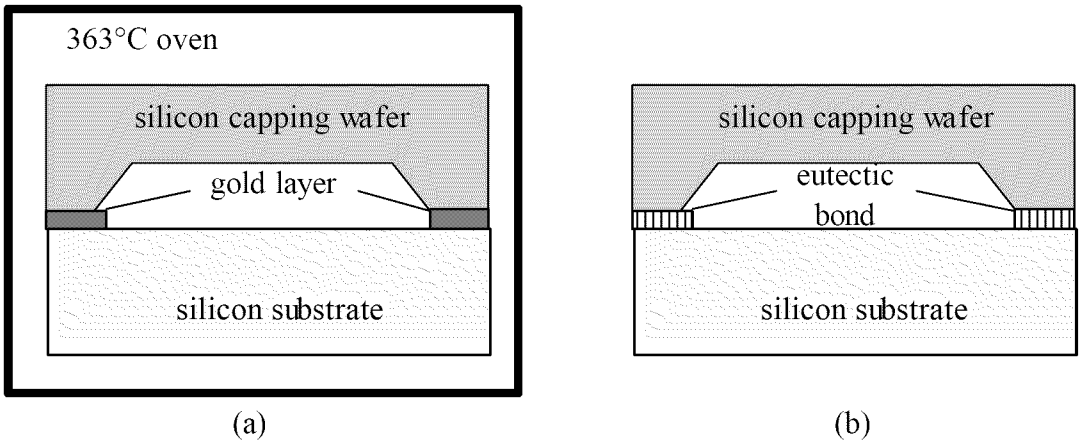


Figure 2.12. Drawing depicting the eutectic bonding process (a) before the eutectic bond forms and (b) after the bond has formed.

2.6.4. Thermocompression Bonding

Another bonding technology is thermocompression bonding. This bonding is achieved by the simultaneous application of pressure and heat between two surfaces that have a metal layer between them at the bonding ring. Ideally a bond would be made by melting the metal at the bonding ring, but the high temperatures required for this would damage the MEMS switch inside the package. Instead the temperature can be reduced to a level where the metal softens and pressure can be applied to the wafers to form a thermocompression bond. Figure 2.13 shows a thermocompression bond being formed between two wafers with gold between them. The wafers have a pressure force applied to them, and are situated in an oven at around 300°C. Tsau et al. demonstrated thermocompresson bonding of gold at a temperature of 300°C and a pressure of 7 MPa for wafer bonding [10]. Gold is often chosen as the bonding metal because it resists oxidation,

which would hinder the bonding mechanism. One disadvantage of the process is that it requires high temperatures to achieve strong bonds that are hermetically sealed, especially if the bonding areas have significant surface roughness.

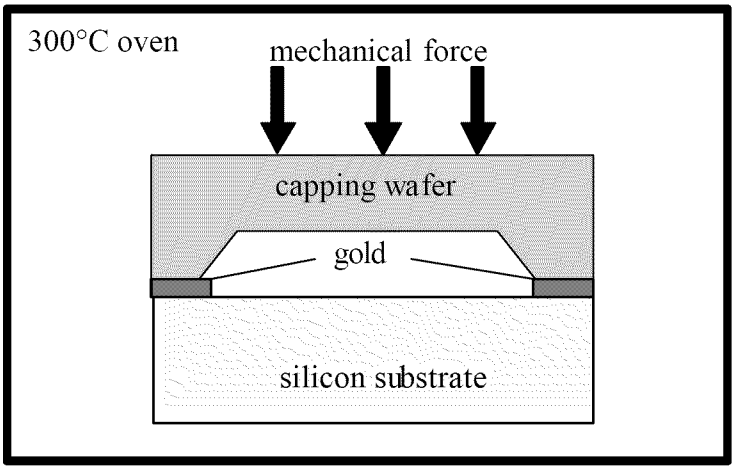


Figure 2.13. Drawing depicting the thermocompression bonding process for wafer bonding using gold as the bonding metal between the wafers.

2.6.5. Solder Bonding

Another bonding method utilizes a solder ring as the bonding agent between the wafers. The bonding process is shown in Figure 2.14. In Figure 2.14(a) the wafers and solder are brought to the melting point of the solder by placing them in an oven. This forms a bond when cooled as shown in Figure 2.14(b). Kim et al. presented a hermetic MEMS package using an AuSn solder ring to bond silicon to silicon [11]. Solder bonding produces a reliable hermetic seal, but the wafers must be heated to the melting point of the solder which is 400°C for AuSn solder. Other solder compounds allow the bonding to occur at lower temperatures due to their lower melting points. Tilmans et al. present a variation of solder bonding by using solder reflow to create the seal [7]. Their method also exploits the surface tension of molten solder to self-align the encapsulations with the

device wafer. This process is known as the indent reflow sealing (IRS) technique. The main disadvantages of solder bonding techniques is the potential outgassing from the solder into the encapsulation, which can cause the switch to degrade in performance or fail by adhering in the "down" position. Other than the potential for outgassing, methods using solder reflow show much promise for MEMS switches due to the low temperatures necessary and the hermetic seal it provides.

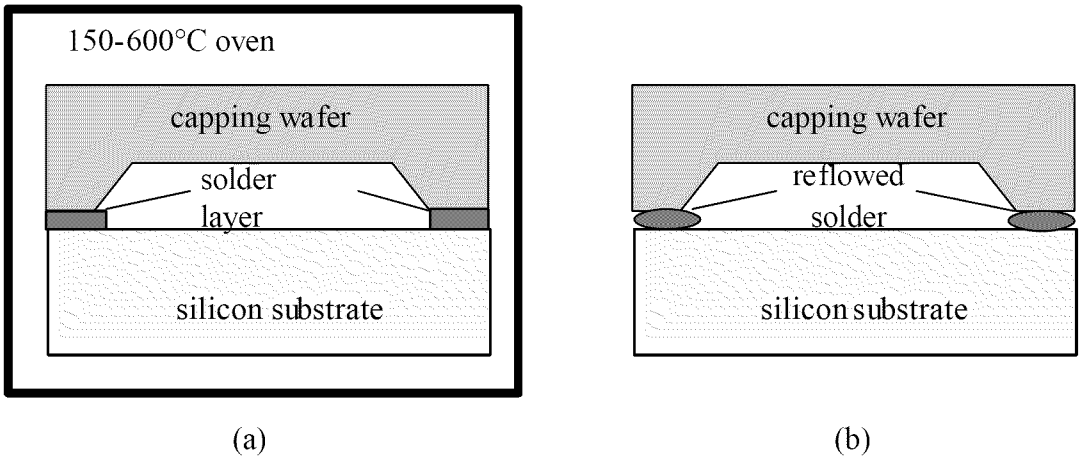


Figure 2.14. Drawing depicting the solder reflow bonding process (a) before the solder was brought to its melting temperature, and (b) after the solder has been reflowed (melted) and cooled.

2.6.6. Epoxy Bonding

Another wafer bonding method uses epoxy or polymers to form the bond, as shown in Figure 2.15. Park et al. bonded a quartz MEMS substrate wafer to a glass capping wafer using a nonconductive B-stage epoxy that was cured at 200°C [12]. Epoxy bonding has the advantage of low curing temperatures (60-200°C), low cost, and high reliability, but has not been shown to produce a fully hermetic seal to date. Since it is generally understood that a hermetic seal is a requirement for reliable RF MEMS switches, epoxy sealing currently doesn't meet their packaging requirements. According

to Rebeiz, some packages produced with this method have been shown to be near hermetic [2]. Further research is necessary on epoxy bonding to determine its suitability for RF MEMS switch packaging. Future research may show that epoxy sealing is a suitable bonding and sealing alternative for the wafer bonding approach to encapsulation.

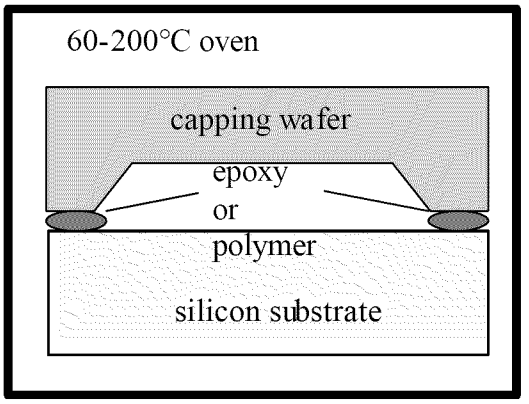


Figure 2.15. Drawing depicting the wafer bonding process using epoxy as the bonding agent between the wafers. The epoxy must be placed in an oven at a relatively low temperature to cure it.

2.6.7. Localized Heating and Bonding

Clearly a common problem among most wafer bonding methods is the high temperature required to form the bonds. This heating is typically achieved by placing the wafers in an oven, which subjects the MEMS devices to high temperatures. Figure 2.16 shows a drawing of the localized heating method. At the bonding ring, resistive microheaters are fabricated through surface micromachining to provide localized heating for the bonding process. Due to the localization of the heating, the MEMS structures are not subjected to high temperatures. Cheng et al. used localized heating to achieve silicon fusion bonding and gold-silicon eutectic bonding [9], silicon-aluminum eutectic bonding [13], and solder bonding [14]. Lin also used localized heating for gold-silicon eutectic bonding, silicon-silicon fusion bonding, and Pb-Sn solder bonding [15]. The localized

heating method has shown to provide hermetic seals of high strength and yield. The main disadvantage of this method is the potential outgassing into the encapsulation from the solder that is typically used for these methods. In addition, it requires the fabrication of microheaters on the substrate wafers whose layout and placement may not be compatible with the MEMS devices on the wafer.

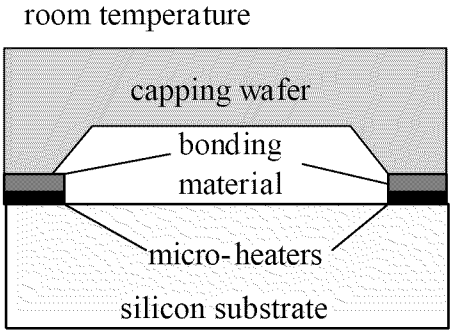


Figure 2.16. Drawing depicting the wafer bonding process using localized heating and bonding. This is accomplished by fabricating and using micro-heaters only on the areas to be bonded, and using one of the several high-temperature bonding methods available. Because the heating is localized to the bonding ring, the MEMS device in the cavity is not subjected to high temperatures.

2.6.8. Summary of Wafer Bonding Techniques

Most of the wafer bonding techniques are very similar, but they use different techniques for the actual bonding and sealing of the wafers. One major disadvantage of wafer bonding techniques is the requirement for a bonding area around each device where the bond is made. This results in a large amount of wafer area being used for the bonding area. This decreases the number of devices that can be fabricated on a wafer, and therefore increases the cost of each device. Another disadvantage of wafer bonding techniques is that packaging is a completely different and separate series of steps from the fabrication of the MEMS structures that are being packaged. When the packaging is done

separately of the device fabrication, it is referred to as post-packaging. The surface micromachining encapsulation method to be discussed next avoids costly post-packaging by integrating the fabrication of the encapsulation with the fabrication of the MEMS devices they are encapsulating.

2.7. Surface Micromachined Encapsulations

The third approach to zero-level packaging of RF MEMS devices is surface micromachining. In this approach, a thin film "shell" is fabricated directly over each MEMS device using similar deposition and patterning techniques that are used to fabricate the switch. The structure is released through etch holes in the encapsulation, and the etch holes are sealed at a desired pressure to ensure a hermetically sealed cavity with a known pressure in the encapsulation.

One of the earliest published realizations of a microfabricated cavity was published in 1990 by Ikeda et al. [16]. In that work, an encapsulation was created around a resonator in order to maximize the resonator's quality factor (Q factor). The cavity that was fabricated was sealed with a pressure of less than 1 mTorr, could withstand 100 MPa of pressure, and had wall thicknesses of 10 µm. This fabrication process was very specialized, and involved five selective epitaxial growth steps, one deposition step, and three selective etch steps.

Lin et al. devised a fabrication process for wafer-level encapsulation that uses standard surface micromachining processes and materials [17]. In their method, a MEMS resonator is first covered with 7 µm of phosphosilicate glass as the sacrificial layer. This layer is then patterned to define the encapsulation. Next, 1 µm of silicon-rich silicon nitride is deposited as the encapsulation shell over the sacrificial layer, with etch holes de-

fined in it to enable release of the sacrificial layers. Next, the sacrificial layers are etched away in a bath of concentrated hydrofluoric acid (HF). The wafer is then cleaned and dried using a supercritical CO_2 dryer. In the supercritical CO_2 drying process, the liquid used in the last step of the release step is replaced directly by CO_2 gas to prevent the surface tension of the fluid from drawing the parts of the MEMS switch together as the fluid evaporates. This surface tension would draw the MEMS switch into the down position where it would be permanently stuck, and therefore useless. Finally, 2 μm of low-stress nitride is deposited with low pressure chemical vapor deposition (LPCVD) to seal the etch holes. This deposition is done at low pressure in order to create a low-pressure encapsulation for optimal (high Q) resonator performance. Further research has been performed Liu and Tai on the use of chemical vapor deposition CVD) methods for the sealing of microcavities [18]. Their study covered deposition methods, sealing materials, and seal performance.

Another surface micromachined encapsulation method uses epitaxially grown polysilicon as the encapsulation layer [19]. This method not only can provide a hermetic seal, but is also very durable to better protect the MEMS device from standard handling and packaging that will occur after encapsulation. Epitaxial silicon was chosen as the encapsulant because of its mechanical strength and ease of deposition and patterning. This process is not suitable for MEMS switches due to the high temperatures required during epitaxial silicon growth (~1000° C). Sealing of the etch holes in the encapsulation was performed by depositing a low temperature oxide (LTO).

Although the earliest realizations of surface micromachined encapsulations for MEMS devices were being published in the early 1990's, it was not until 2002 that the

first patent was obtained for this technology, by Wood and Dudley. [20]. In this patent, specific materials or processes are not described, but the patent is rather for the general idea of using surface micromaching to encapsulate a MEMS device to protect it from further packaging.

2.7.1. Nickel Electroplated Encapsulations

Stark and Najafi demonstrated another method of producing hermetic packages using a thick layer of electroplated nickel as the encapsulation [21]. This provides a mechanically strong encapsulation, which aids in protecting the device in later packaging steps. Figure 2.17 shows an SEM image of one of their nickel electroplated encapsulations. Etch holes were not defined in the encapsulation, but rather tunnels were defined at points where the encapsulation would have made contact with the substrate. These "fluidic access ports" are later closed at vacuum pressures by reflowing prefabricated micro lead-tin (Pb-Sn) solder balls over the entire encapsulation. This method was shown to result in a hermetic seal; however the fact that the entire encapsulation is made of metal would not lend itself well to encapsulating RF MEMS switches. The large extent of metal that makes up the encapsulation and the minimal gap between the encapsulation and the signal lines going into and out of the encapsulation would contribute to large parasitic capacitances between the signal line and the encapsulation, resulting in poor RF performance. One possible variation on their method in order to improve RF performance would be to construct part of the encapsulation with a dielectric and part of it with metal. The reduced extent of metal would decrease the parasitic capacitance and therefore improve RF performance. The use of a dielectric structural layer for the encapsulation was not considered by the authors, but was considered in this thesis.

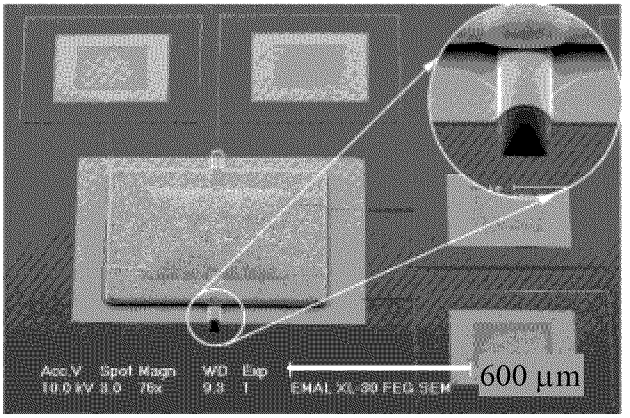


Figure 2.17. SEM image of a MEMS encapsulation fabricated by electroplating nickel over a sacrificial layer (over a MEMS device). The sacrificial layer is etched away through the "fluidic access ports" on the sides of the encapsulation, and the access ports are sealed through various methods. [21].

2.7.2. Permeable Polysilicon Encapsulation

A variation on surface micromachined encapsulation techniques is the use of porous polysilicon as the encapsulation layer. When thin layers of polysilicon are deposited under certain conditions of temperature, doping, and pressure, they have a porous structure that is permeable to HF, a common etchant used to release MEMS devices. Porous polysilicon has a mesh structure of pores with radii of 5-20 nm. Lebouitz et al. used "windows" of permeable polysilicon in an otherwise non-permeable polysilicon encapsulation to allow release of a MEMS resonator through the encapsulation [22]. Figure 2.18 shows side cut-away drawings of the key steps in their encapsulation process. In Figure 2.18(a) the encapsulation frame with etch access windows is fabricated over a sacrificial layer and the porous polysilicon is fabricated over the entire structure. Next, in Figure 2.18(b) the sacrificial layer is etched away directly through the porous polysilicon windows. Finally, in Figure 2.18(c) a sealing layer that does not penetrate the porous polysilicon layer is fabricated over the encapsulation, which seals the porous windows.

The porous polysilicon windows were amply large for the HF to perform a complete release of the PSG sacrificial layer, but were small enough that they were easily sealed by LPCVD silicon nitride layer without the silicon nitride entering the cavity and corrupting the MEMS resonator. This encapsulation technique seems to work well for polysilicon resonators, but is not suitable for RF MEMS switches due to the high temperatures that are necessary to deposit the polysilicon and porous polysilicon (> 600° C).

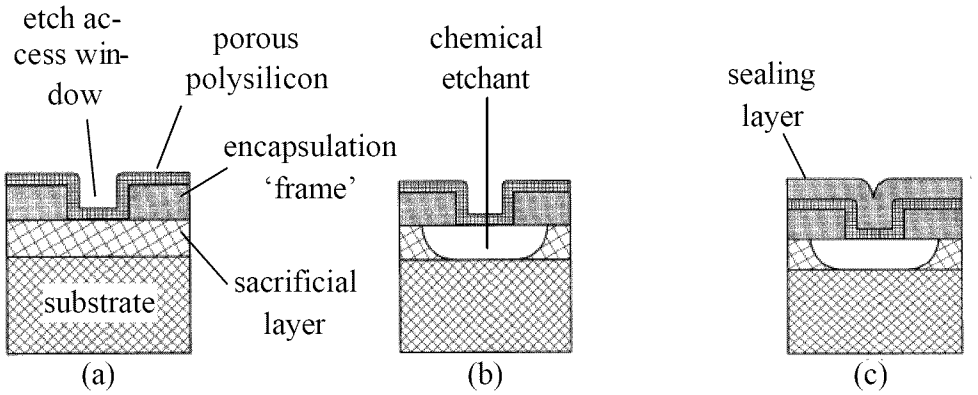


Figure 2.18. Side cut-away drawings of the encapsulation process using porous polysilicon etch access windows; (a) the encapsulation frame with etch access windows is fabricated over a sacrificial layer and the porous polysilicon is fabricated over the entire structure; (b) the sacrificial layer is etched away directly through the porous polysilicon windows; (c) a sealing layer that does not penetrate the porous polysilicon layer is fabricated over the encapsulation, which seals the porous windows. [22].

2.7.3. AFRL Encapsulation Process

The AFRL RF MEMS switch whose fabrication process is shown earlier in Figure 2.4 is the basis for the AFRL encapsulation process. The encapsulation process requires only a few more surface micromachining steps, using similar sacrificial and structural materials as were used to fabricate the switch.

The process starts with unreleased switches as shown in Figure 2.19(a). The first step, shown in Figure 2.19(b) is to deposit 2-3 μm of PMGI (an electron-beam resist) and

pattern it with photoresist over the entire unreleased switch. These encapsulation "forms" are next reflowed at 250°C to create rounded sidewalls. In the next step, shown in Figure 2.19(c), 1-2 μm of silicon nitride is deposited by sputtering or low pressure chemical vapor deposition (LPCVD). This layer is patterned over the sacrificial layer to create an encapsulation over each switch using optical resist as the etch mask. Next, etch holes are patterned in each encapsulation and etched with reactive ion etching (RIE) or wet chemical etching. In Figure 2.19(d) the next step is shown to be the release of the encapsulation and the switch through a soak in PMGI stripper. Immediately following the release, the switches are dried using a CO_2 critical point dryer to avoid stiction. In the final step, shown in Figure 2.19(e) the etch holes are sealed using one of a variety of methods that are still under investigation. An annotated SEM image of the AFRL capacitive switch with a dielectric encapsulation can be seen in Figure 2.20, showing all dimensions. To verify that the encapsulated switch was completely released, the encapsulation was torn away for inspection inside the encapsulation. Figure 2.21 shows an SEM image of the switch with the dielectric encapsulation partially torn away. The image shows that the MEMS switch and encapsulation were completely released through the etch holes in the encapsulation.

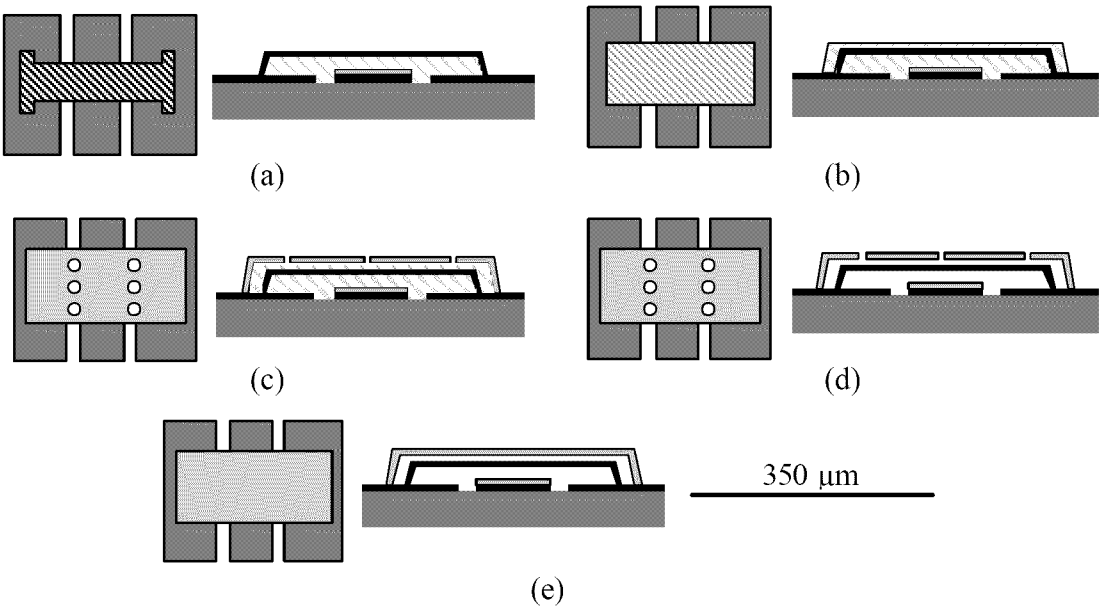


Figure 2.19. Top and side cut-away drawings of a step-by-step fabrication process for RF MEMS switch encapsulation based on the AFRL encapsulation process; (a) begin with unreleased switch; (b) deposit and pattern second sacrificial layer over entire MEMS switch, and reflow; (c) deposit encapsulation dielectric over sacrificial layer and pattern it with etch holes in it; (d) release switch and encapsulation with a wet chemical etch through the etch holes; (e) seal the etch holes in the encapsulation layer to create a sealed encapsulation. Note: the vertical dimension is exaggerated for clarity.

To create sealed encapsulations, the etch holes must then be sealed. This sealing cannot introduce material into the encapsulations because the switch performances may be affected. The exact material and process that will be used to seal the holes is the subject of ongoing research by AFRL and the author. Some materials that are being considered are spin-on glass and thermal/UV cured epoxies. Wu et al. have performed a thorough evaluation of electrical and mechanical performance of nonhermetic commercial conformal coatings for MEMS encapsulation including silicone elastomers, epoxies, and Parylenes [23]. They characterized moisture ingress resistance, mobile ion permeation, and adhesion of the materials when used for encapsulation. Another idea that is the subject of this research is to use a metallization layer over each encapsulation to seal the

etch holes. A metal layer may have the added advantages of providing some electromagnetic shielding and physical durability to the encapsulation. Another advantage of a metal sealing layer is that it is known to provide a hermetic seal, whereas polymers and epoxies often do not provide a hermetic seal.

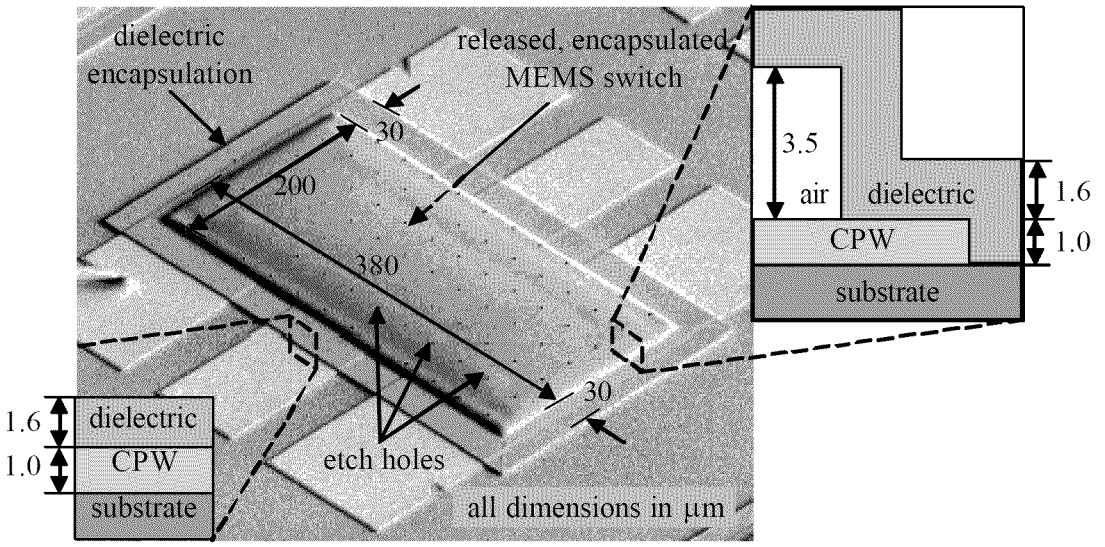


Figure 2.20. Annotated SEM image of an AFRL RF MEMS switch with a dielectric encapsulation fabricated over it. Also included are side cut-away views to show the vertical dimensions [5].

It has already been discussed that the requirements for RF MEMS encapsulation are that it must provide protection for each MEMS device from physical damage and contamination during further packaging, it must not take up too much area on the wafer, and it must provide a hermetically sealed cavity for the switch to operate in. One other requirement that has not been discussed yet is for the encapsulation to ideally have no negative effects on the switch's performance.

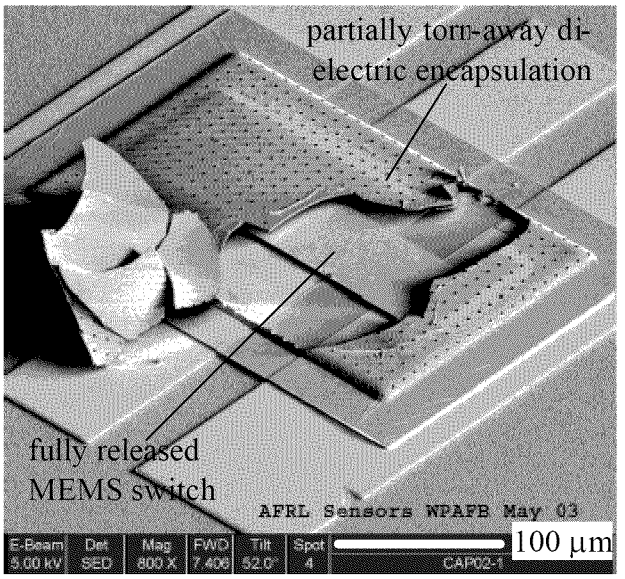


Figure 2.21. Annotated SEM image of an AFRL RF MEMS switch with a dielectric encapsulation that has been partially torn away to show that the encapsulated switch was completely released through the etch holes in the encapsulation [5].

2.8. Performance Characterization of RF Switches and Packaging

An important factor in the design of zero-level packaging is the effect on the high frequency performance of the RF switch. Scattering parameters are commonly used to characterize microwave networks, and are thoroughly explained by Pozar in his familiar text [24]. The scattering parameters for RF MEMS switches are used to characterize their performance, and are also used to characterize the effect of the packaging on the performance of the switch. Next, scattering parameters will be described, as well as how they are used to characterize the performance of a microwave switch.

2.8.1. Scattering Parameters

For an n-port network, the scattering parameters (S-parameters) are given in a scattering matrix, or [S] matrix, that has the dimensions of n by n. The value of each element S_{ij} is a complex value describing a voltage wave at port i when port j has a voltage wave incident on it. All ports other than port j are assumed to have loads on them that are

impedance matched to the microwave network so they will not have any effect on ports *i* and *j*. Also, the incident waves on all ports other than the *j*th port are set to zero. Consider a two-port network because it accurately describes an electrical switch. Figure 2.22(a) shows a drawing of a two-port network, with the *S*-matrix that describes the performance of the network. The four *S*-parameters for a two-port network are illustrated in Figure 2.22(b) and described below:

- S_{11} is the reflection coefficient at port 1. A voltage is attached to port 1, a matched load is attached to port 2, and the reflected voltage wave at port 1 is measured.
- S_{21} is the forward transmission coefficient (from port 1 to port 2). A voltage is attached to port 1 and the voltage is measured at port 2.
- S_{12} is the reverse transmission coefficient (from port 2 to port 1). A voltage is attached to port 2 and the voltage is measured at port 1.
- S_{22} is the reflection coefficient at port 2. A voltage is attached to port 2, a matched load is attached to port 1, and the reflected voltage wave at port 2 is measured.

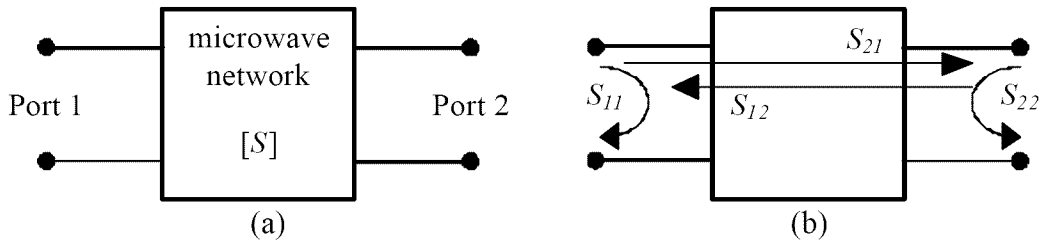


Figure 2.22. (a) Illustration of a generic 2-port microwave network that can be described by *S*-parameters in the *S*–matrix [S]; (b) simplified diagram of the four S-parameters for a 2-port network.

These concepts can easily be extended to any *n*-port network. In symmetrical network, which usually describes RF MEMS switches, the reflection coefficient at port 2 (S_{22}) is identical to the reflection coefficient at port 1 (S_{11}) and the reverse transmission coefficient (S_{12}) is identical to the forward transmission coefficient (S_{21}).

S-parameters can be calculated analytically based on voltage or current waves incident to a network, and they can be easily measured in a laboratory using a vector network analyzer.

2.8.2. Insertion Loss

One of the most important metrics for characterizing the performance of a RF switch (or other electrical components) is insertion loss. Insertion loss is a measure of the loss introduced into a system, and is formally defined in dB by Pozar [24] with

$$IL = -20\log|T| \tag{2.1}$$

where T is the transmission coefficient, which can easily be found from the more familiar reflection coefficient Γ with

$$T = 1 + \Gamma \tag{2.2}$$

where

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.3}$$

where Z_L is the impedance of the network and Z_0 is the characteristic impedance of the transmission line feeding the network. Alternatively, in practice the *S*-parameters are used to calculate insertion loss:

$$IL = 20\log|S_{21}| \tag{2.4}$$

In this formulation, the insertion loss is given in negative dB, where a lossless network will have an insertion loss of 0 dB and a network that completely attenuates the incoming signal has an insertion loss of -∞ dB. The insertion loss of a capacitive RF MEMS switch is measured with the switch in the up state (closed circuit).

2.8.3. Return Loss

Another important performance metric for microwave networks is return loss. Return loss is the ratio in dB of the incident power to the reflected power from a network. The formal definition is simply the dB value of the reflection coefficient, Γ:

$$RL = -20\log|\Gamma| \tag{2.5}$$

Alternatively, in practice the *S*-parameters are used to calculate the return loss:

$$RL = 20\log|S_{11}| \tag{2.6}$$

Here the return loss is again given in negative dB. In general for microwave networks, it is desirable to minimize the return loss, so ideal networks have a return loss of -∞ dB using Equation (2.6). The return loss of a capacitive RF MEMS switch is measured with the switch in the up state (closed circuit).

2.8.4. Isolation

Isolation is a measure of the performance of a switch when it is in the down, (open circuit) state. It is a measure of the signal that "leaks" through a switch, and is calculated from the *S*-parameters with:

$$Isolation = 20\log|S_{21}| \tag{2.7}$$

The isolation as calculated here is again a negative number. An ideal switch will have an isolation of -∞ dB using Equation (2.7).

2.8.5. Microwave Effects of Packaging on RF MEMS Switches

There are four main issues that determine the high-frequency characteristics of the zero-level package:

- The parasitic and reflection losses at the encapsulation boundary due to the RF feed-throughs into and out of the encapsulation

- The parasitic losses in the transmission line due to proximity coupling with the encapsulation
- The losses from the detuning of the transmission line (impedance mismatch) due to the encapsulation and switch
- The losses due to the lossy dielectric that makes contact with the transmission line at the feed-throughs of the encapsulation

The effects of these mechanisms on microwave performance are shown in the insertion loss, return loss, and isolation of the network. An ideal switch adds no losses or reflections to the network when in the closed-circuit state and perfectly blocks all signals from propagating through it when in the open-circuit state. Although excellent RF MEMS switches have been designed, and some suitable zero-level packaging methods have been developed, rarely is the RF performance of the package a factor when designing the package.

Various researchers have looked into the RF performance of packaging using the flip-chip (wafer bonding) packaging method. Park et al. used RF vias from the backside of the capping wafer to minimize detrimental RF effects of the packaging [12]. Margomenos et al. studied RF performance of wafer bonded packaging through modeling and measurement [25]-[27]. Margomenos and Katehi have characterized the parasitic losses due to the RF feed-throughs, metallic bonding ring, and DC bias lines in [25]. In other research, Margomenos et al. paid special attention to the RF transition into the package [27]. Holzman et al. developed a multi-layer ceramic feed-through for microwave multi-chip modules in their research [28]. In [29] Other related research by Jourdain et al. provided a thorough analysis on optimizing the performance of the entire package as part of the design process [29]. Extensive testing and modeling is done in the paper, and again it

is based on wafer bonded packages. Another treatment on optimizing the RF performance of the package was performed by Hwang et al., however it is focused on conventional ceramic packages (Level 1 packaging), and its intent is more on evaluation of off-the-shelf packaging rather than on design and optimization [30]. DeMarco et al. paid special attention to microstrip and CPW transitions into high frequency hermetic packages that employed LTCC (low temperature co-fired ceramic) as the capping layer with a metallization ring as the sealant [31].

2.9. Summary

The motivation for RF MEMS switches was introduced by describing current RF switches, based on semiconductors, in Section 2.1. Next, in Section 2.2 the field of MEMS is introduced, including how they are fabricated. In Section 2.3 RF MEMS switches are described, including how they work and their advantages and disadvantages. In Section 2.4 a particular challenge of RF MEMS, packaging, is described. In Sections 2.5 and 2.6, conventional packaging and wafer bonding approaches to packaging MEMS are described, including their advantages and disadvantages. In Section 2.7, a third approach to MEMS packaging is described: surface micromachining. Also described in this section is the AFRL encapsulation process that is the basis for this thesis research. Finally, in Section 2.8 figures of merit for RF MEMS switches are described. Also in this section is a literature survey of research in designing and characterizing packaging for RF MEMS switches. The next chapter presents the novel encapsulation designs that were created for performance analysis and optimization in subsequent chapters of this thesis.

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3. Encapsulation Designs

Several different encapsulation designs were created for analysis and testing. Most designs were not created before analysis and simulation of electrical performance began; rather the test matrix was expanded with new designs after each previous design was analyzed. In this manner, new designs could be created and analyzed based on the knowledge gained from analyzing previous designs, and the overall performance could be optimized based on knowledge learned in the iterative design-analyze-design cycle.

3.1. Capacitive RF MEMS Switch Geometry

Each encapsulation was designed over a capacitive RF MEMS switch whose geometry and dimensions are shown in Figure 3. In Figure 3.1(a), a top view drawing of the switch is shown, with all major designable dimensions denoted. In Figure 3.1(b) a side cut-away view of the same switch is presented. Also included is a blow-up of the center section of the switch so the layer thicknesses and air gap width can be denoted. The corresponding dimensions for the switch that was encapsulated and analyzed in this work is shown in Table 3.1.

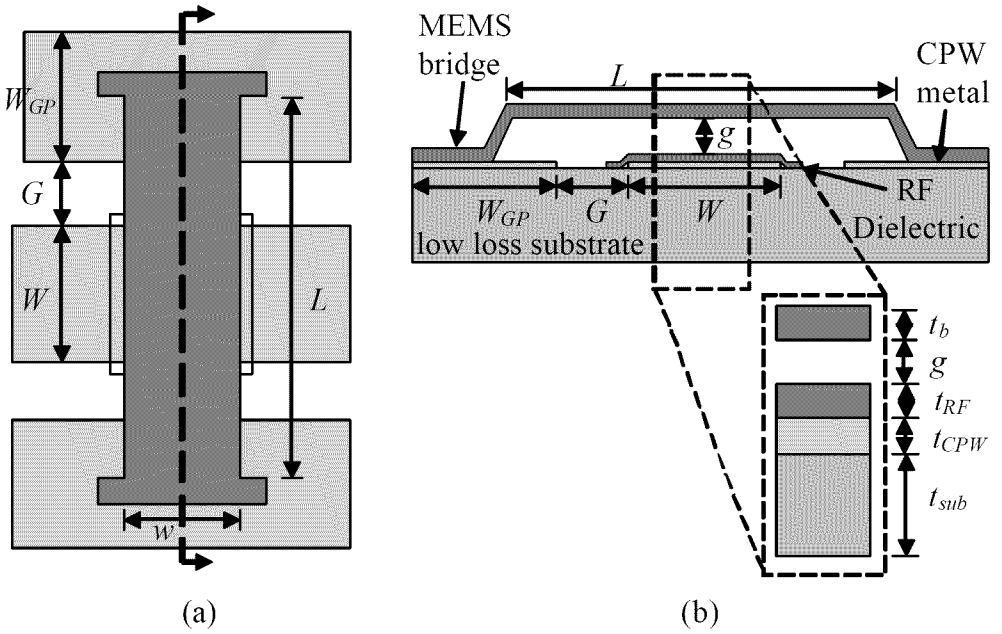


Figure 3.1. (a) Top view and (b) side cut-away drawings of the capacitive RF MEMS switch that is encapsulated in this work. Note: the vertical dimension is exaggerated for clarity.

Table 3.1. Dimensions of the capacitive RF MEMS switch that was encapsulated in this work.

Parameter	Symbol	Value (μm)
Beam length	L	300
Beam width	w	120
Beam thickness	t_b	0.7
Air gap	g	3.5
RF dielectric thickness	t_{RF}	0.2
CPW thickness	t_{CPW}	0.3
CPW signal width	W	80
CPW ground width	W_{GP}	120
CPW gap width	G	40
Substrate thickness	t_{sub}	432

3.2. Encapsulation Design Geometries

Encapsulations were designed as the zero-level package for the RF MEMS switch described above. In Figure 3.2(a) a top view of the encapsulation is shown, and a side cut-away drawing is shown in Figure 3.2(b).

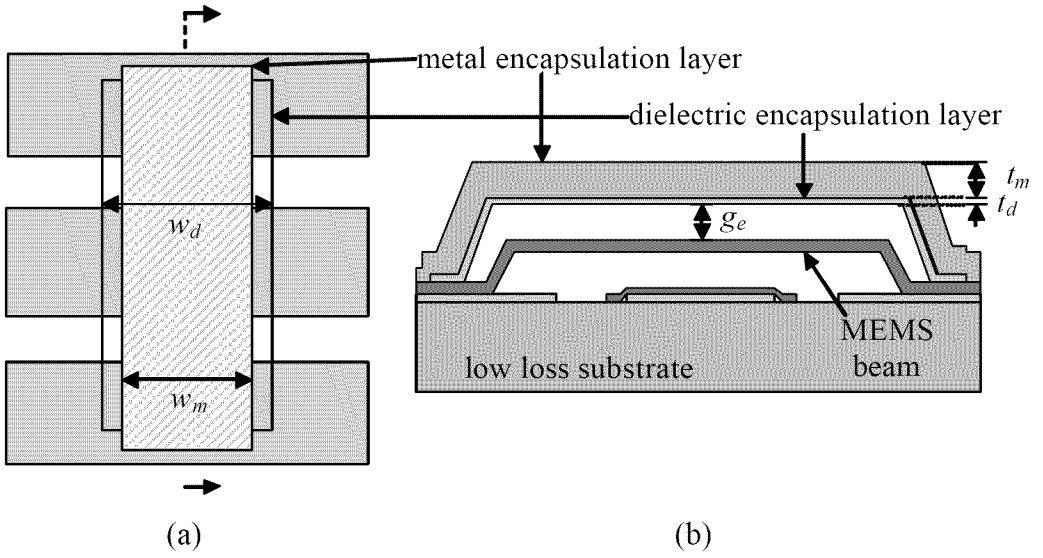


Figure 3.2. (a) Top view and (b) side cut-away drawings of the encapsulated capacitive RF MEMS switch, showing the geometry variables that are varied in the different designs. Note: the vertical dimension is exaggerated for clarity.

The parameters that were varied in the encapsulation designs were the metal layer width w_m, the dielectric layer thickness t_d, and the air gap between the switch and the encapsulation g_e. The geometries for the entire design space are shown in Table 3.2. A detailed list of each design configuration is given in Table 3.3.

Table 3.2. Summary of the dimensions of the encapsulation designs. Note that the metal layer width, w_m, the dielectric layer thickness, t_d, and the air gap between the switch and the encapsulation, g_e, are all parameters that were varied in the different designs.

Parameter	Symbol	Value (μm)
Dielectric layer width	w_d	200
Metal layer width	w_m	160 - 214
Dielectric layer thickness	t_d	1.6 - 3.2
Metal layer thickness	t_m	5.0
Air gap between switch and encapsulation	g_e	3.5 - 6.5

Table 3.3. Description of geometry of all encapsulation designs. The designs are further subdivided into two configurations based on the state of the MEMS switch, up or down. For every configuration, the dielectric encapsulation width w_d is 200 μm and the metal layer thickness is 5.0 μm.

Design #	Config. #	Switch state	Metal layer width, w_m	Dielectric layer thickness, t_d	Encapsulation air gap, g_e	Modified RF feed-through
1	1U	Up	None	None	3.5	No
	1D	Down				
2	2U	Up	None	1.6	3.5	No
	2D	Down				
3	3U	Up	160	1.6	3.5	No
	3D	Down				
4	4U	Up	200	1.6	3.5	No
	4D	Down				
5	5U	Up	214	1.6	3.5	No
	5D	Down				
6	6U	Up	214	3.2	3.5	No
	6D	Down				
7	7U	Up	200	1.6	5.0	No
	7D	Down				
8	8U	Up	180	1.6	3.5	No
	8D	Down				
9	9U	Up	200	1.6	6.5	No
	9D	Down				
10	10U	Up	214	3.2	3.5	Yes

In designs 5 and 6, the metal layer is wider than the dielectric layer. Figure 3.3(a) shows a top view of the encapsulation in this case. The side cut-away view of this encapsulation better shows the dimensions of this case. Note that the width of the dielectric layer (w_d) is actually the width of the raised part of the dielectric encapsulation layer, not of the entire layer. It does not include the part of the layer that rests on the substrate (or CPW), which is a 20 μm pad on all sides of the raised encapsulation. The metal layer does not have a pad around it, so the metal layer width (w_d) includes the full width of the

metal layer. Therefore, in the designs where the metal layer width is wider than the dielectric layer width, the metal layer is prevented from making electrical contact with the RF signal line by the dielectric encapsulation layer pad around the encapsulation.

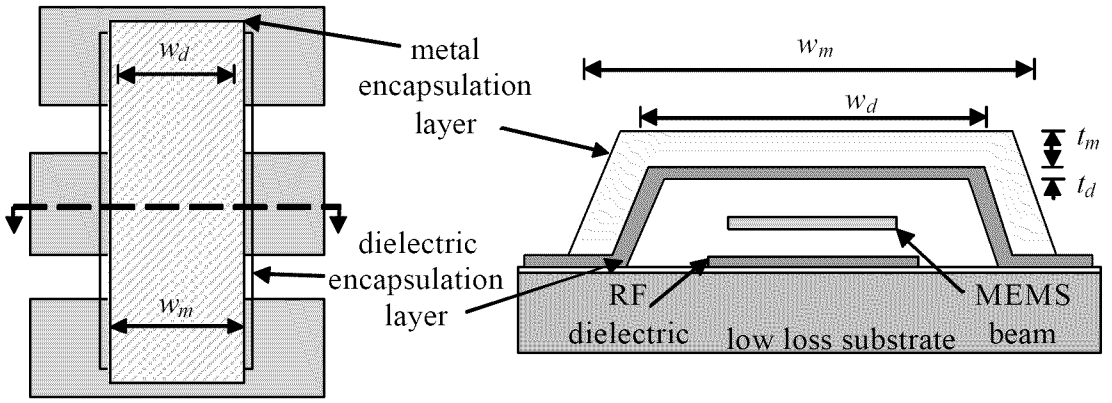


Figure 3.3. Top view and side cut-away drawings of an encapsulated capacitive RF MEMS switch, showing the structure of design configurations 5 and 6, where the width of the metal encapsulation w_m is greater than the width of the dielectric encapsulation layer w_d. Notice that w_d is not the entire extent of the dielectric layer, but only the part of it that forms the raised encapsulation. Note: the vertical dimension is exaggerated for clarity.

In every design with a metal layer, the dielectric layer is designed with a void in the 20 µm pad directly above the two CPW ground traces. This electrical contact makes the metal layer of the encapsulation electrically grounded. This grounding has several advantages for the packaging that will be discussed later in this document.

3.3. RF Feed-Through Design

In design 10, an RF feed-through for the transmission line into and out of the package was designed to minimize the detrimental effects of the package on the overall RF performance. In the design, the encapsulation design was identical to design 6, but the CPW signal line width was modified to a width W_H over a length L_H. The transition was centered on the edge of the encapsulation where the dielectric and metal layers conform

down to the CPW signal line. A top view drawing of this geometry is shown in Figure 3.4, and the dimensions of the RF feed-through are given in Table 3.4. The theory behind the RF feed-through design is given in Chapter 4.

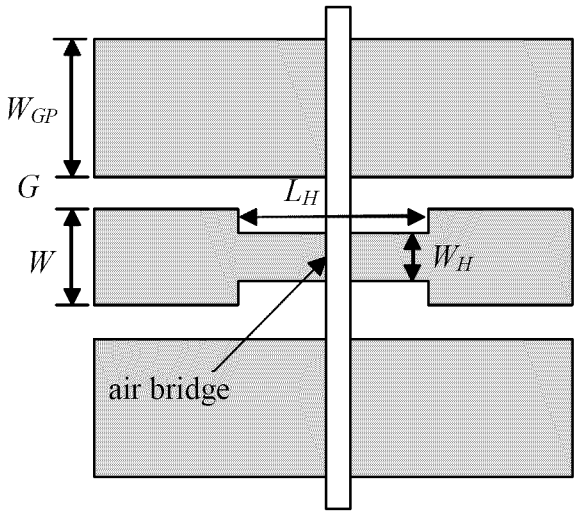


Figure 3.4. Overhead drawing of the RF feed through design dimensions. The CPW width is modified for a length of LH/2 on each side of the feed-through to impedance match the feed-through to the transmission line.

Table 3.4. Numerical values for the geometry parameters of the CPW signal line modification for the RF feed-through design.

Parameter	Symbol	Value (μm)
CPW signal line width at feed-through	W_H	44
Length of RF feed-through segment	L_H	37.5

3.4. Material Properties

For the analytical modeling described in Chapter 4 and the electromagnetic simulation described in Chapter 5, the material properties of the materials in the substrate, switch materials and encapsulation materials are needed. The materials that were used in fabricating the switches and encapsulations are known, and the property values for these materials were obtained from published sources [1]-[4]. However, the exact values for

these properties were not obtained experimentally. Because the property values for many materials often vary with each fabrication run, the values below are a potential source of error on the modeling and simulation results in comparison to the test data.

Table 3.5. Material properties for each material in the RF MEMS switch and encapsulation. These values are used for analytical modeling and electromagnetic simulation.

Property, units	Symbol	Value	Reference
Substrate: R-plane sapphire	-	-	-
Relative permittivity	$\varepsilon_{r,sub}$	9.4	[1]
Dielectric loss tangent	$\tan \delta_{sub}$	0.001	[1]
CPW lines and MEMS beam: gold	-	-	-
Bulk conductivity, MS/m	σ_b	45.5	[2]
RF dielectric: alumina	-	-	-
Relative permittivity	$\varepsilon_{r,RF}$	9.2	[3]
Dielectric loss tangent	$\tan \delta_{RF}$	0.008	[3]
Encapsulation dielectric: silicon nitride	-	-	-
Relative permittivity	$\varepsilon_{r,d}$	7.0	[4]
Dielectric loss tangent	$\tan \delta_d$	0.001	[4]
Encapsulation metal: indium	-	-	-
Bulk conductivity, MS/m	σ_m	12.5	[2]

3.5. Summary

In this chapter the encapsulation designs that were created for performance analysis were described. The encapsulation designs include a dielectric layer that is partially covered by a metal layer. The variable dimensions are the thickness of the dielectric layer, the width of the metal layer, and the height of the encapsulation. The theory that is used to model the RF performance of these encapsulations is presented in the next chapter. Also, the design of a RF feed-through into the encapsulation is presented, and the modeling of its performance is presented in the next chapter.

3.6. References

[1] Liang, G., R.S. Withers, B.F. Cole and N. Newman, "High-temperature superconductive devices on sapphire," *IEEE Transactions on Microwave Theory and Techniques,* vol. 42, pp. 34-40, 1994.

[2] Source: WebElements [http://www.webelements.com/].

[3] Rebeiz, G.M., *RF MEMS Theory, Design, and Technology,* Hoboken, NJ: Wiley-Interscience, 2003.

[4] Madou, M.J., *Fundamentals of Microfabrication,* Boca Raton, FL: CRC Press, 2002.

4. Analytical Modeling

It is necessary to use microwave circuit theory rather than standard circuit theory to analyze a circuit when the dimensions of the circuit are on the order of a wavelength of the signal involved. Standard circuit theory, based on lumped elements, can be thought of as an approximation of electromagnetic theory as described by Maxwell's equations. However, lumped element circuit models can be developed for analysis of microwave systems if they are based on the unique phenomena that occur at higher frequencies. In particular, parasitic capacitances, inductances, and resistances must be considered when developing the high-frequency lumped-element equivalent circuit models. These principles are applied here in developing lumped element equivalent circuit models for RF MEMS switches and their encapsulations. The RF performance of these circuits was then determined through the use of a software microwave circuit simulator [1].

4.1. RF MEMS Switch Equivalent Circuit Model Development

A capacitive RF MEMS switch can be modeled with a lumped-element equivalent circuit model as shown in Figure 4.1. In this model, the air gap between the bridge and the CPW signal line creates a variable capacitor (C_b) with two states: a small capacitance in the up state due to the relatively large air gap, and a larger capacitance in the down state. For the current that couples to the bridge, the path to either ground plane of the CPW is half the length of the bridge, resulting in an equivalent inductance (L_b) and resistance (R_b). Further explanation for this model along with the theory used to calculate the numerical values for each element are described below. In this model it is understood that the CPW that the switch is built on has a characteristic impedance Z_0 and the losses due to the transmission line are very small due to the very short length of transmission line

that is considered. Because of this, transmission line losses are not considered. The values for the lumped elements in the analytical model were developed without the aid of the results from the full-wave simulations or laboratory testing. It may be possible to "tweak" some of the parameters of the analytical models in order to make them match up closer to the full-wave simulation data and test data, but the intent of this model was to produce data based on parameters from published data and not to produce a model based on data fitting.

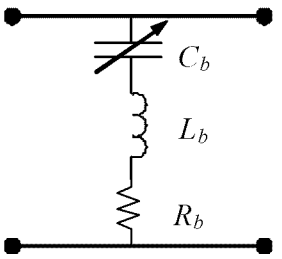


Figure 4.1. Lumped-element equivalent circuit schematic for a capacitive RF MEMS switch.

In this model, the bridge forms a series RLC circuit, and the impedance of the bridge, Z_b is

$$Z_b = R_b + j\left(\omega L_b - \frac{1}{\omega C_b}\right) \tag{4.1}$$

where ω is the angular frequency of the RF signal, and C_b is the bridge capacitance, which is either the up state capacitance C_u or the down state capacitance C_d. When the imaginary component of Z_b is zero, the circuit is at a resonant frequency. Setting the imaginary part of Equation (4.1) equal to zero, and also knowing that $\omega=2\pi f$, where f is the RF frequency, leads to an expression for the resonant frequency f_0,

$$f_0 = \frac{1}{2\pi\sqrt{L_b C_b}} \tag{4.2}$$

According to Muldavin and Rebiez [2], the impedance of the switch can be approximated by

$$Z_b = \begin{cases} \dfrac{1}{j\omega C_b}, & \text{for } f << f_0 \\ R_b, & \text{for } f = f_0 \\ j\omega L_b, & \text{for } f >> f_0 \end{cases} \tag{4.3}$$

Therefore the switch can be approximated as a capacitor below the resonant frequency and as an inductor above the resonant frequency. A well designed switch will have the down state resonant frequency aligned with the RF signal design frequency to maximize the isolation of the switch. The resonant frequency of most capacitive switches in the up state is typically much greater than the RF signal frequency, so its impedance can be modeled as a capacitor. This fact makes modeling very intuitive and straightforward, because the capacitance is relatively simple to model using simple formulas. In the following sections, accurate values for the capacitances are developed and described.

4.1.1. Up-State Capacitance

Capacitive RF MEMS switches depend on high-frequency electromagnetic coupling between the suspended bridge and the CPW signal line to create a low impedance state, or near-short-circuit state, from signal to ground when the bridge is actuated downward onto the RF dielectric. When the bridge is not actuated, the air gap between the bridge and the signal results in very small electromagnetic coupling between bridge and signal line, resulting in a high impedance, or near open circuit state, between the signal line and the bridge. This variable electromagnetic coupling can be modeled in a

lumped element equivalent circuit as a variable capacitor with two states: up capacitance C_u and down capacitance C_d. An approximation for C_u and C_d can be obtained using the parallel-plate capacitor calculation:

$$C_{pp} = \frac{\varepsilon A}{d} \tag{4.4}$$

where ε is the permittivity of the medium between the conductors, A is the overlapping area of the parallel plates, and d is the distance between the plates. In the case of the RF MEMS switch shown in Figure 3.1, A is calculated by the width of the MEMS bridge (w) multiplied by the width of the CPW signal line (W). In the down state, d is replaced with the thickness of the RF dielectric (t_{RF}), and ε is replaced by the permittivity of free space (ε_0) multiplied by the dielectric constant (relative permittivity) of the RF dielectric (ε_{RF}).

In the up state, the gap between the conductors is filled with two different diectrics, air and the RF dielectric, as shown in the simplified drawing in Figure 4.2(a). The parallel plate capacitance can be calculated as a series combination of two capacitors, one for each medium. The capacitance of the air filled area uses the air gap width g as the distance separating the parallel plates, and the medium has a relative permittivity of 1. The parallel plate capacitance is then calculated with

$$C_g = \frac{\varepsilon_0 w W}{g} \tag{4.5}$$

The capacitance across the RF dielectric uses the thickness of the RF dielectric layer (t_{RF}) as the distance between the plates, and the relative permittivity of the RF dielectric in the calculation. The capacitance across the RF dielectric is given by

$$C_{RF} = \frac{\varepsilon_0 \varepsilon_{RF} w W}{t_{RF}} \tag{4.6}$$

The total up state capacitance is calculated from the series combination of C_g and C_{RF} as shown in Figure 4.2(b), and can be simplified to a single capacitance C_u as shown in Figure 4.2(c) and calculated with

$$C_u = \frac{\varepsilon_0 w W}{g + \frac{t_{RF}}{\varepsilon_{RF}}} \tag{4.7}$$

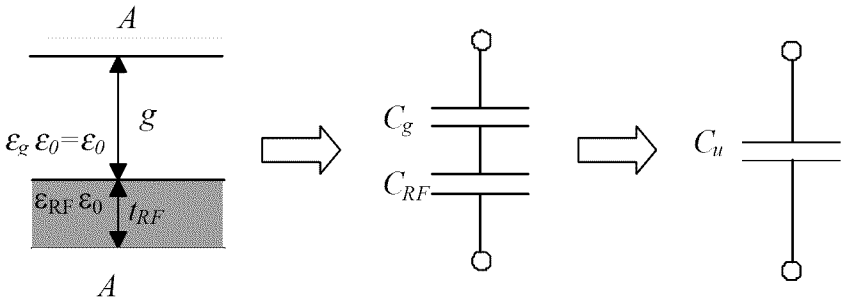


Figure 4.2. (a) Simplified drawing of the geometry of the beam and CPW signal line overlap area used for parallel plate capacitance calculation; (b) series capacitors that model the geometry's capacitance; (c) total capacitance of switch in up state from calculation of two capacitors in series

In the up state, the simple parallel plate capacitance calculation is not very accurate because it neglects all fringing field capacitance. To explore the actual fringing field capacitance, the capacitance was calculated using Coventorware, a commercial finite element modeling (FEM) software package [3]. In particular, the MemCap module was used to solve for capacitance between the MEMS bridge and CPW signal line. First a 3-dimensional solid model of the MEMS switch was built in Coventorware. Next, the solid model was meshed and the capacitance between the bridge and signal line was extracted

using a numerical simulation. All of the setup and analysis settings that were used in Coventorware are presented in Appendix A. The difference between the parallel plate approximation result and the FEM result is the amount of fringing field capacitance, and it is expressed as a percentage of the parallel plate approximation value. The result was the fringing field capacitance increased the total capacitance value from the parallel plate calculation by 45%. This value agrees with published data from Muldavin and Rebeiz for fringing field capacitance of similar RF MEMS switches [2].

The capacitance values for each switch configuration, with adjustments from the parallel plate approximation for the fringing field capacitance in the up state and surface roughness in the down state (described in the next section) were computed by writing a simple computer program. The code from the program is presented in Appendix B. The values calculated by this program are given in Table 4.1, and are what were used as the capacitance values in the equivalent circuit model.

4.1.2. Down-State Capacitance

In the down state, the fringing field capacitance is neglected in this model. Wong et al. showed that in the down state fringing fields are very small compared to the overall capacitance because of the very small distance between the conductors in the down state [4]. However, in the down state the parallel plate capacitance calculation overestimates the actual capacitance because of surface roughness that is inherent in the RF dielectric layer from fabrication. If a contact area of 50% of the bridge and RF dielectric overlap area are assumed, along with a perfectly flat RF dielectric layer and a surface roughness of 100 Å, values published by Muldavin and Rebeiz show that the actual capacitance is only 60% of the parallel plate approximation [2]. This calculation of taking 60% of the

parallel plate capacitance approximation value is what was used for the bridge capacitance for all design configurations in the down state.

Table 4.1. Calculated capacitance values for the bridge and encapsulation for all design configurations. These values are what were used for the capacitors in the lumped element equivalent circuit model.

Config. #	Capacitance, Parallel Plate, [fF]	Adjustment in Bridge Capacitance due to Fringing Fields	Adjustment in Encap. Capacitance due to Fringing Fields	Adjustment in Beam Capacitance due to Surface Roughness (SR)	Effective Capacitance, [fF]
1U	24.14	+45%	0%	0%	35.20
1D	3910.00	0%	0%	-40%	2346.00
2U	24.14	+45%	0%	0%	35.20
2D	3910.00	0%	0%	-40%	2346.00
3U	27.71	+45%	+20%	0%	39.50
3D	3916.00	0%	0%	-40%	2354.00
4U	31.28	+45%	+20%	0%	43.77
4D	3923.00	0%	0%	-40%	2361.00
5U	72.91	+45%	+20%	0%	85.57
5D	3965.00	0%	0%	-40%	2404.00
6U	52.32	+45%	+20%	0%	64.93
6D	3944.00	0%	0%	-40%	2382.00
7U	30.15	+45%	+20%	0%	42.40
7D	3920.00	0%	0%	-40%	2358.00
8U	29.50	+45%	+20%	0%	41.62
8D	3920.00	0%	0%	-40%	2358.00
9U	41.00	+45%	+20%	0%	41.41
9D	3918.00	0%	0%	-40%	2355.00

4.1.3. Bridge Inductance

The MEMS bridge presents an inductance in series with a resistance due to the current that is coupled to it from the signal line, and then flows to the CPW ground planes. Because the capacitance of the bridge in the up state is very small, and therefore the current in the bridge is very small also, the inductance of the bridge has very little ef-

fect on the switch performance, and can be neglected. In the down state however, most of the current in the CPW signal line couples to the bridge and flows through the bridge, so the inductance is important. Equation (4.2) shows that the bridge inductance is an inversely proportional to the resonant frequency f_0, so it is a very important contributor to the switch isolation.

It is very difficult to calculate an inductance value of the bridge, so the value used in this model is extrapolated from test inductance data from Muldavin and Rebiez for capacitive RF MEMS switches of nearly the same geometry as the one considered in this research [2]. The value used for L_b in this model is 5.0 pH.

4.1.4. Bridge Resistance

The resistance of the bridge is also a significant factor in the switch performance in the down state, and can be neglected in the up state. The resistance can be calculated from the cross-sectional area of the bridge and the resistivity of the bridge metal with

$$R_b = \frac{1}{2}\frac{\rho_b(L_b/2)}{wt_b} \tag{4.8}$$

In this calculation, skin depth effects are neglected. The effect of skin depth is that as the signal frequency is increased the effective resistance of the bridge also increases. A larger bridge resistance results in lower isolation and higher return loss, both undesirable.

Using the geometry of the switch and the bulk resistivity of gold, the switch resistance for this model was calculated to be 0.02Ω, and is the value used in all design configurations.

4.2. Encapsulated RF MEMS Switch Equivalent Circuit Model Development

Similar to the switch itself, an encapsulation with a grounded metal layer can be modeled as a series RLC circuit. This series RLC segment is oriented similarly to the switch model: shunted from signal to ground. Together these two RLC segments are oriented in parallel to each other, as shown in Figure 4.3.

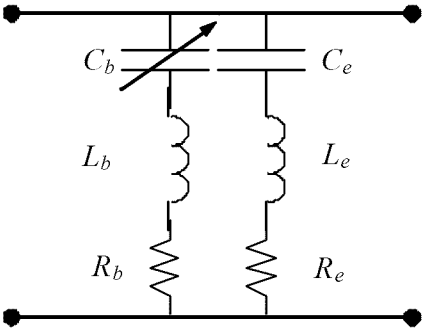


Figure 4.3. Lumped-element equivalent circuit schematic for a capacitive RF MEMS switch and encapsulation with a metal layer.

In design 2, the encapsulation consists entirely of a dielectric layer with no metal layer on top of it. The analytical model developed here does not calculate the losses due to a dielectric encapsulation. It can safely be assumed that the effects on the switch due to a dielectric encapsulation are minimal, so when comparing data results later in this work, the unencapsulated switch model data is also used for the dielectric encapsulated switch designs.

4.2.1. Encapsulation Inductance and Resistance

The encapsulation is similar to the MEMS bridge in the up state, although the encapsulation does not deform downward like the bridge does. The encapsulation in most of the design configurations is further away from the CPW signal line, so the resulting capacitance is smaller than the MEMS bridge in the up state, which is already very small.

This results in a very high resonant frequency, which means we can approximate it with a capacitor only. For these reasons, the encapsulation resistance and inductance can be neglected. In encapsulation designs 5 and 6, the metal layer of the encapsulation is closer to the CPW signal line than the MEMS bridge, but its width is very small compared to the width of the MEMS bridge, so the same assumptions will be used for designs 5 and 6 also (approximate it only with a capacitance).

4.2.2. Encapsulation Capacitance

Since encapsulation inductance and resistance can be neglected, the remaining encapsulation capacitance is now in parallel with the beam capacitance. To find the overall capacitance from the beam and encapsulation, the capacitances are simply added since capacitors in parallel can be combined with simple addition.

The parallel plate capacitance approximation is again the starting point for calculating the capacitance of the encapsulation. For designs 3-4 and 7-9, where the width of the metal encapsulation (w_m) is less than the width of the dielectric encapsulation (w_d) the width of the upper plate is calculated as the overlap width of the encapsulation over the bridge below it. For example, in design 3 the width of the metal encapsulation is 160 μm and we know the width of the MEMS bridge is 120 μm, so the overlap width used for the parallel plate approximation is 40 μm. As before, the width of the other "side" of the plate used to calculate the plate area is the width of the CPW signal line, W.

To increase the accuracy of the parallel plate approximation, fringing field capacitance was added to the calculation. A solid model of design 5 (w_m=160 μm) was created and analyzed in Coventorware. The result was that the total capacitance between the CPW signal line and the MEMS bridge and encapsulation was 39.5 fF. We already know

the total capacitance of the bridge alone is 35.2 fF, so the added contribution from the metal encapsulation is 4.3 fF. The parallel plate capacitance approximation yields a capacitance of 3.57 fF, so the added contribution from fringing field capacitance is 0.8 fF, or about 20% of the parallel plate approximation value. This 20% fringing field adjustment was used for all of the metal encapsulation layer capacitance calculations.

For encapsulation designs 5 and 6, the capacitance due to the upper part of the encapsulation (on top of the raised encapsulation) is calculated as explained in the previous paragraph. The width used is the width of the dielectric encapsulation (w_d) plus twice the thickness of the dielectric encapsulation layer (t_d). This value is then adjusted to account for 20% additional capacitance due to fringing fields as before. This capacitance is added to the contribution from the metal sidewalls, explained next.

For the part of the metal layer that conforms down the sidewalls onto the dielectric "pad" around the encapsulation, the capacitance is calculated separately. In the designs, it s assumed that the width of metal that conforms down onto the dielectric pad is the thickness of the metal encapsulation layer. At points directly above the signal line, the signal line and the grounded metal encapsulation layer are only separated by the thickness of the dielectric encapsulation layer (t_d). The parallel plate approximation is used to calculate capacitance here, with the dimensions of the parallel plate being the thickness of the dielectric layer (t_d) and the width of the CPW signal line, W. Zero fringing field capacitance is also assumed due to the small distance separating the conductors. No adjustment was made for surface roughness, and fringing field capacitance due to the sidewalls of the metal layer was neglected. This capacitance is then added to the contribution from the upper part of the metal layer to arrive at the total capacitance for the encapsulation.

4.3. Electrical Performance Extraction from Analytical Models

Ansoft Designer SV (Student Version) [1] was the microwave circuit simulator that was used to extract the RF performance from the equivalent circuit models. This software application was chosen because it is accurate and easy to use. In addition, because it is a student version, it is downloadable for free to anyone. The student version of the software has no limitations in it over the full version that affected the analysis required for this research. This software outputs *S*-parameter data, which is what is needed for comparison to test and simulated data.

The circuit simulation process was fast and simple. First the lumped element circuit schematics were created in the software, and the values for the circuit elements were entered. Next, a frequency sweep was set up to analyze the circuit from 1 to 40 GHz at intervals of 0.1 GHz. After analysis, the data was exported to a data file for plotting.

4.4. RF Feed-Through Design and Analytical Model

After completion of analysis on designs 1-9 (as described in Table 3.3), another design was created that put special attention on the RF feed-through of the CPW signal line into and out of the encapsulation. In particular, design 6 (w_d=200 μm, w_m=214 μm, t_d=3.2 μm, g_e=3.5 μm) was considered for modification. In this design the metal layer extended beyond the width of the dielectric encapsulation and conformed down the sidewalls of the encapsulation onto the dielectric pad below it. This design was considered for improvement because if it were possible to create a high-performance encapsulation design where the metal extended beyond the dielectric encapsulation on all sides, it would simplify the fabrication of the encapsulation by allowing the metal layer to act as an etch mask for the dielectric encapsulation layer below it. By applying impedance

matching techniques, the RF performance (insertion loss and return loss) can theoretically be improved. Designs 5 and 6, where the metal encapsulation is physically close to the CPW signal line but the RF feed-throughs are not engineered (not impedance matched), can be considered as the worst-case scenarios for RF feed-through performance. By applying impedance matching techniques, the feed-through performance can be improved over designs 5 and 6. The encapsulation designs themselves are not altered; only the CPW signal line is modified to increase performance.

Consider a CPW with characteristic impedance Z_0. For this analysis, we will consider only the RF feed-through section of the encapsulation, and will assume we can impedance match to the transition, independent of the rest of the encapsulation and the MEMS beam. This region is similar to a metal air bridge of width W_{AB} and height t_d. From these dimensions a parallel plate capacitance C_{AB} is calculated. This capacitance leads to coupling between the air bridge and the CPW signal line, contributing to insertion loss. In terms of impedance, the air bridge has the effect of decreasing the impedance of the transmission line. This impedance mismatch leads to poor return loss performance. In other words, the impedance discontinuity causes reflections of the RF signal back into the circuit which is generally undesirable.

In this design, the dimensions of the transmission line are modified in order to increase the characteristic impedance of the line around the RF feed-through region. This is done to compensate for the parasitic capacitance from the feed-through into the encapsulation that decreases the characteristic impedance of the line. Figure 4.4 shows a top view drawing of the geometry of the CPW around an air bridge as presented by Weller et al. [5].

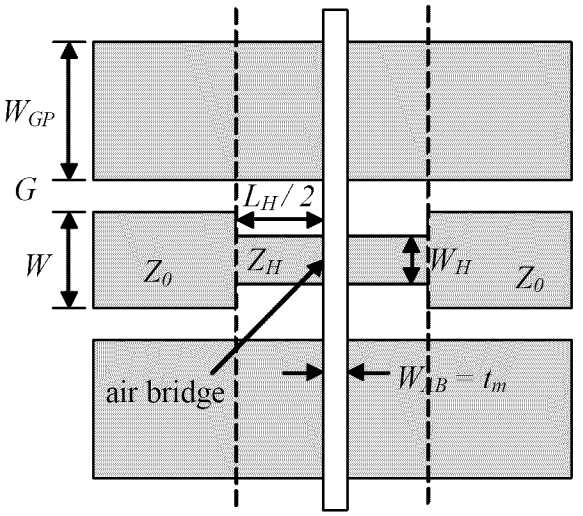


Figure 4.4. Overhead view drawing of an impedance matched RF feed-through under an air bridge. The design uses a high-impedance CPW segment of impedance Z_H and of length $L_H/2$ on each side of the air bridge to compensate for the low impedance condition caused by the air bridge. The air bridge is suspended above the CPW signal line by a distance t_d, and is electrically connected to the CPW ground planes.

Using CPW analysis equations from the text by Simons [6], the center conductor was narrowed in order to create a high impedance line with impedance Z_H=70 Ω. The effective dielectric constant for the high impedance segment, ε_{re}, is calculated with the design equations in [6], and was found to be 5.17. These design equations from [6] and the computer code that was written to make these calculations is presented in Appendix C. The resulting center conductor width, W_H, in the high impedance region was 44 μm. The ground plane traces were not modified. Weller et al. preset a design equation for the required length of the high impedance section, L_H.[5]. This equation is based on ideal transmission line theory. The required length for an impedance match with the air bridge is given by

$$L_H = \frac{c}{\sqrt{\varepsilon_{re}}} \frac{Z_H Z_0^2 C_{AB}}{Z_H^2 - Z_0^2} - 0.7 W_{AB} \tag{4.9}$$

where c is the speed of light and C_{AB} is the parallel plate capacitance between the air bridge and the signal line, and ε_{re}, W_{AB}, Z_H, and Z_0 were defined earlier. Equation (4.9) is valid, assuming

$$\tan\left(\frac{\theta}{2}\right) \approx \frac{\theta}{2}$$
$$Z_H \omega C_{AB} << 1 \tag{4.10}$$

where θ is the electrical length of the high impedance section in radians and ω is the angular frequency corresponding to the RF signal frequency. The feed-through capacitance (C_{AB}) was calculated from the parallel plate capacitor formula to be 4.3 fF. The other required values for the given scenario (Z_H=70 Ω, Z_0=50 Ω, ε_{re}=5.17) along with C_{AB} were used in Equation (4.9) to arrive at the length of the high impedance section, L_H=37.5 μm. The conditions in (4.10) were met, so the theory could be applied in this situation.

In [5] the length of high impedance transmission line (L_H) is centered on the air bridge. In order to apply this theory to the encapsulation geometry, half of the length is used at each feed-through into or out of the encapsulation. A screen image of the design from HFSS is shown in Figure 4.5. This design was simulated in HFSS, and the results are shown in Chapter 7.

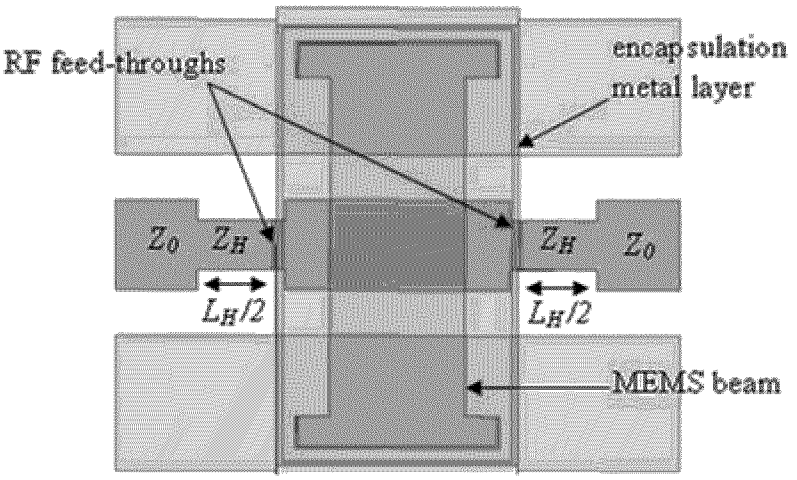


Figure 4.5. Overhead drawing of the RF feed-through design. The high impedance CPW segment is impedance matched to the air bridge of the transition area into the encapsulation. RF feed-through under an air bridge. Note: the metal encapsulation layer and MEMS bridge are semi-transparent in this drawing.

The lumped-element equivalent circuit model was also modified to account for the high-impedance segment in the transmission line. A CPW center conductor width step change can be modeled by a series inductor with a value of L_{step} with theory presented by Rebeiz [7]

$$L_{step} \cong \frac{Z_H (L_H / 2)\sqrt{\varepsilon_{re}}}{c} \tag{4.11}$$

where L_{step} is the inductance of the step change (not a physical or electrical length), and Z_H, L_H and ε_{re} are the same as defined earlier. The equivalent inductance found from Equation (4.11) and used in the analytical model was 9.9 pH. The modeled performance of the feed-through is presented in Chapter 7. Also, the computer code that was written and used to make these calculations is presented in Appendix C.

4.5. Modeling of Metal Reflow Over Etch Holes

A key step in fabricating the encapsulations is to reflow the metal layer across the etch holes to seal them shut. It is necessary for the width of the etch hole and the thick-

ness of the metal layer to meet certain criteria in order to guarantee that the metal will reflow across the etch holes when brought to its liquid state. Consider a metal layer of thickness t_m with a square etch hole in it with a width of w_{eh}. If the thickness is many times greater than the hole width, intuitively the hole will close when the metal brought to its liquid state. On the other hand, if the metal thickness is very small compared to the hole width, the hole has no chance of closing. Somewhere in the middle exists a critical metal thickness at which the metal must be as thick as or thicker than to guarantee the hole will close when reflowed.

The physical phenomenon that governs metal reflow is surface tension of fluids. The necessary etch hole width in relation to the metal thickness in order to guarantee hole closure was determined using an open source surface tension modeling code known as The Surface Evolver, written by Brakke [8]. The Surface Evolver is a program for the study of surfaces governed by surface tension and other energies. On the scale of MEMS, gravitational forces are negligible, so the only forces that were considered in this research were surface energies. Given an initial surface or volume geometry in a data file, Surface Evolver meshes the surface into triangular elements, and interactively evolves the surface until a minimum energy state is achieved. The minimum energy state for a volume of liquid is the state that a volume of solder will take on after being reflown, so the software can be used effectively to model this situation. The Surface Evolver output used for this research was a 3-D graphical representation of the evolved surface.

To analyze the reflow of a layer of solder with an etch hole it using Surface Evolver, several simplifying assumptions were made. The first assumption is that solving the problem with a square hole with dimension w_{eh} will give the same results as if the

problem were solved with a round hole of diameter w_{eh}. The second assumption is that the solder will not wet the inside of the hole in the dielectric layer below it. In other words, the solder will only change shape around the etch hole in the process of achieving its minimum energy state, it will not be drawn into the hole because the solder is drawn into the hole due to the solder wetting the inside of the hole. The final assumption is that the solder surface has been prepared by flux if necessary, and so it reflows freely. A cleaned solder surface will not have oxides that have formed on it that would prevent it from reflowing freely or wetting to itself.

A Surface Evolve data file was set up to analyze a section of the metal encapsulation layer with a single hole in the center of it, as shown in Figure 4.6. This data file (which is the "code" that Surface Evolver analyzes) is presented in Appendix D. It is assumed that this section of solder is one in an array of many similar sections. Because of this, the outer faces of the volume are fixed in the data file; that is, Surface Evolver will not evolve their surfaces due to surface forces. In addition, the bottom face of the volume is fixed, for obvious reasons. The faces that will evolve are the top face and the four faces that make up the sides of the etch hole. With slight modifications to the data file, different ratios of width to thickness can quickly and easily be modeled and evolved to determine if the hole will close or not for those dimensions. For this analysis, the hole width was fixed and the metal thickness was varied until a critical thickness was determined. The metal layer must meet or exceed this critical thickness for the given etch hole width to guarantee hole closure. This critical thickness was determined for etch hole widths of 3 μm and 5 μm, and the results are presented in Chapter 7.

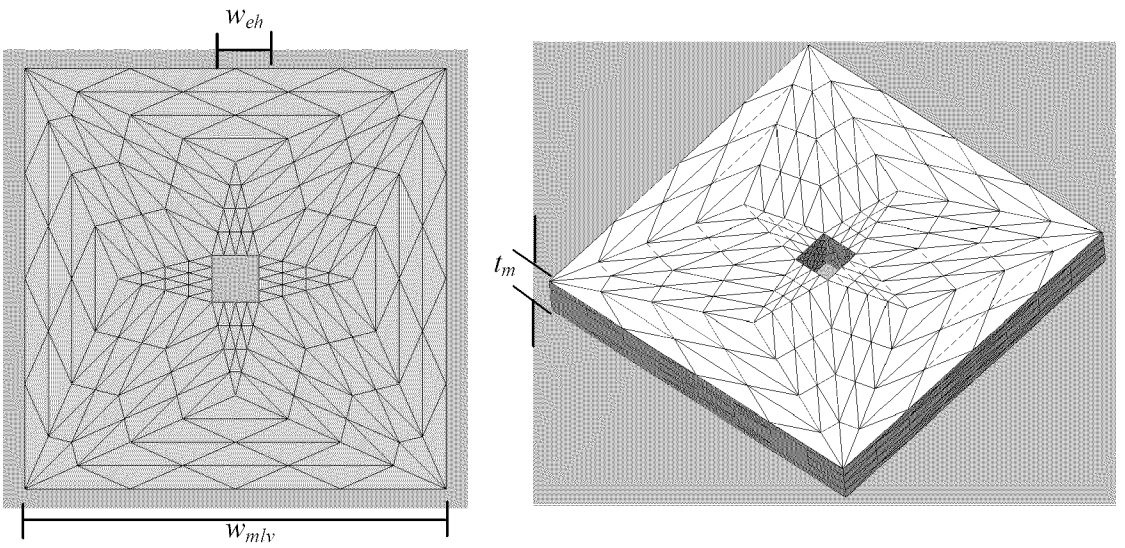


Figure 4.6. Surface Evolver graphical output showing the geometry of the volume of solder that was the starting point for iterating on to see of the etch hole in the center will close when the volume is brought to a liquid state. Here, the etch hole width, w_{eh}, is fixed at 5 µm, the length of one edge of the volume, w_{mlv}, is 40 µm, and the hole is centered in the volume. The metal layer thickness, t_m, is varied in the analysis.

4.6. Summary

In this chapter the theory behind the analytical model for the RF MEMS switch and its encapsulation was developed, as well as the theory behind the RF feed-through design. It was shown that the electrical performance of the structures can be modeled using a lumped element equivalent circuit. Also, the methodology for modeling solder reflow over the etch holes was presented. The other methods for analyzing the electrical performance of the RF MEMS switch and encapsulation are presented in Chapter 5 (simulation) and Chapter 6 (testing). All data is compared and discussed in Chapter 7.

4.7. References

[1] Ansoft Designer Student Version, version 1.0, Ansoft Corporation, 2003

[2] Muldavin, J. B. and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches—part I: modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp.1045-1052, Jun. 2000.

[3] Coventorware, version 2001.3, Coventor Corporation, 2001.

[4] Wong, C. H., M. J. Tan, and K. M. Liew, "Electrical characterization of RF capacitive microswitch," *Sensors and Actuators A*: Physical, vol. 102, pp. 296-310, Jan. 2003.

[5] Weller, T. M., R. M. Henderson, K. J. Herrick, S. V. Robertson, R. T. Kihm, and L. P. B. Katehi, Three-dimensional high-frequency distribution networks – part I: optimization of CPW discontinuities," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp.1635-1642, Oct. 2000.

[6] Simons, R. N., *Coplanar Waveguide Circuits, Components, and Systems*, New York: Wiley-Interscience, 2001.

[7] Rebeiz, G.M., *RF MEMS Theory, Design, and Technology*, Hoboken, NJ: Wiley-Interscience, 2003.

[8] Brakke, K. A., *Surface Evolver Manual*, version 2.20, Susquehanna University, Aug. 2003.

5. Full-Wave Finite Element Electromagnetic Simulation

The analytical models developed in Chapter 4 are useful tools for quickly assessing the performance of encapsulations, but in order to make them simple enough to be usable they are based on several simplifications and assumptions. These simplifications and assumptions have the effect of reducing the accuracy of the models. Typically, the accuracy of analytical models is assessed by comparing the model data to test data. Another source of accurate data for electromagnetics is known as full-wave simulation, which is a form of computational electromagnetics. In full-wave simulation, the structure to be assessed is geometrically discretized into elements, and the overall fields, waves or currents are determined by solving the fields, waves, or currents on (or due to) each element. The algorithms used to calculate the fields and waves are using fundamental electromagnetic theory based on Maxwell's equations. Therefore, the theory and mathematics required for full-wave simulation can be quite complex, but also can be very accurate. The largest source of error in these finite element analyses is due to the refinement (or lack of refinement) of the mesh of the structure. Although an extremely fine mesh leads to very accurate results, it also requires a large amount of computing time. It is not unheard of to have computing times on the order of days or weeks, even on very fast computers. Often supercomputers are used to perform these analyses. For this reason, effort is made to mesh the structure fine enough to get accurate results, but not to mesh it to the point where the computing time is unreasonable, or not to the point where mesh refinements will incur much additional computing time with only limited improvement in accuracy.

5.1. Description of Software Tool Used

Ansoft HFSS (High Frequency Structure Simulator) [1] was used as the software package to perform the full-wave electromagnetic simulations. This product was chosen for several reasons. First, HFSS is widely used and accepted for high-frequency analysis of MEMS. Examples of recent MEMS papers for MEMS analysis are from Muldavin and Rebeiz [2] and Wong et al. [3]. Second, HFSS has a very intuitive user interface and, so a new user doesn't have to spend a lot of time learning how to use the program. Finally, the product is offered at a steep educational discount, making it feasible to purchase for this project.

HFSS uses the finite element method to generate an electromagnetic field solution. In the finite element method, the problem space is divided into many smaller regions, known as elements, and the field in each one of these regions is calculated. In HFSS, the element type used is a tetrahedron, a four-sided pyramid. The collection of all elements is called the finite element mesh.

To generate the field solution, the field quantities at the vertices (also called nodes) and at the midpoints of the edges of each tetrahedron are calculated. The values of the field quantities at locations inside the tetrahedron are interpolated from the vertices. A first-order basis function is used, resulting in 20 unknowns per tetrahedron. In this manner, the problem space is discretized, and Maxwell's equations can be transformed into matrix equations that can be solved with numerical methods.

5.2. How to Get Started in HFSS

To get started in using the software tool, the following general steps must be followed:

1. Start the program and open a new project. Within the project create a new design. Select the Solution Type "Driven Modal" for RF MEMS analysis.

2. Create the solid model of the structure using the built in computer-aided design (CAD) tool. Complex structures are created by uniting, subtracting, and intersecting basic structures. For each structure, name it, assign a material to it, and input the necessary material properties for it.

3. Select the faces of your structure that will be ports and define them as "Wave Ports."

4. Add a Solution Setup (under Analysis) and define the solution parameters. Default values can be used for a first cut at the solution, but the parameters will later need to be modified to achieve higher accuracy.

5. Add a frequency sweep to the Solution Setup. Define the frequencies to be analyzed, and the step size.

6. Validate the design by clicking on the Validation Check button. Make any changes to the model and setup that are necessary to pass validation.

7. Analyze the design by clicking on the Analyze button.

8. When the analysis is done, right-click on Results and select Solution Data. Under the Convergence tab the number of tetrahedra used and the convergence data is presented. Under the Matrix Data tab the S-Parameters, impedance, and reflection coefficients for each frequency can be viewed and exported to a data file.

9. Any of the solution data can be viewed and compared in plots by right-clicking on Results and selecting Create Report.

10. Any of the fields and currents can be viewed and animated by selecting the structure, right-clicking on it, and selecting Plot Fields.

Detailed explanations for every aspect of setting up, running, and examining results for an HFSS simulation can be found in the HFSS online help that comes with the software.

5.3. Input of Structure Geometries and Material Parameters

The solid models of the structures to be analyzed are created in HFSS's built-in 3-dimensional CAD tool. In addition to the geometry of the RF MEMS switch and substrate, an air box must be created above the structure and below the substrate to define the problem area where the fields are calculated. An image of the solid model of the unencapsulated switch and the problem area is shown in Figure 5.1. In the figure we see the MEMS device on the substrate, and the air boxes above and below the substrate. The wave ports are also labeled in the figure, and their functionality will be described in the next section.

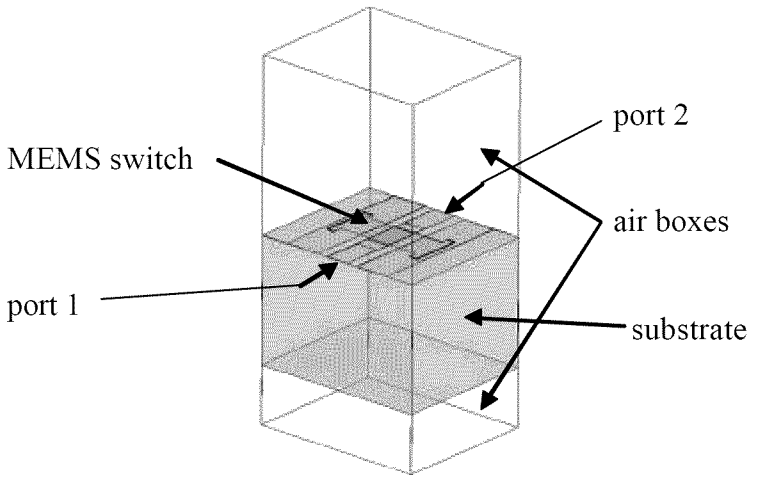


Figure 5.1. Image from HFSS of the solid model for the unencapsulated switch including the entire problem area that was defined for analysis. The excitation ports are also shown; each port encompasses the entire face of the solid model that the end of the CPW touches.

5.4. Definition of Excitations and Boundaries

At the boundaries of the defined problem area, a grounded perfect electric conductor (PEC) boundary is set up, so no energy can enter or exit through it. It is for this reason that the problem area must be defined to be much wider than the CPW width, and

why the air boxes must be included above and below the structure. If the problem area is defined to be too small, the electric fields on the CPW would go from the signal line to the sidewalls of the problem area instead of to the CPW ground planes as they should.

Also shown in Figure 5.1 are the locations of the excitation ports. On each end of the CPW, a wave port is defined as the excitation port. Wave ports define the plane through which signals enter and exit the structure being analyzed. HFSS assumes the structure is attached to an infinitely long waveguide of the same dimensions of the port. Wave ports override the PEC boundary condition defined for the other boundaries. The wave ports extend to the edges of the design and problem area, encompassing the edge faces of the upper and lower air boxes, substrate, and CPW. HFSS generates solutions by exciting one wave port at a time with 1 W of time-averaged power while leaving the other port at 0 W.

5.5. Simulation Set-Up Parameters

Several other parameters must be defined before a simulation can take place. First a frequency sweep must be defined. HFSS provides a frequency sweep called an 'interpolating sweep' that offers several benefits over a normal (discrete) sweep when the frequency band is wide and the model behavior is relatively smooth, which are presumed to both be true in this case. In an interpolating sweep, the solution for an entire frequency range is estimated from only a few frequency points. HFSS chooses where these frequency points will be so that the entire solution falls within a specified error tolerance. The full-field solution is only saved at the last frequency point, but the *S*-parameters are saved at every frequency point. The interpolating sweep allows for greatly reduced proc-

essing times but introduces only minimal error in the solutions. The interpolating sweep used for all analysis was a sweep from 1 to 40 GHz, with a step size of 5 GHz.

HFSS performs an iterative mesh refinement on the structure (to be discussed later), but this process may be manually aided by the user by "seeding" the mesh. For this analysis, the CPW lines, the MEMS bridge, and the metal encapsulation layer were seeded to have the longest dimension of the elements no longer than 30 μm. With this setting, the longest element was $1/250^{th}$ the size of the shortest wavelength analyzed (7.5 mm at 40 GHz). Defining a mesh smaller than 25 μm usually caused the simulation to fail because the computer would run out of memory while solving the solution matrix.

5.6. Adaptive Solution Parameters and Process

The HFSS solution process adaptively refines the mesh of the structure and calculates the *S*-matrix of a structure in the following steps:

1. The structure is discretized into a finite element mesh.
2. If the user chooses, the mesh is refined so that the element lengths are at most a fraction (the Lambda Refinement parameter) of the wavelength.
3. Any seeding of the mesh as defined by the user is performed.
4. The 2-D mesh (triangles) of the ports is iteratively refined until it meets user defined error criteria (Port Field Accuracy)
5. The modes (field patterns) at each port are calculated at the designated solution frequency. The modes that are supported are those that would be supported by a long transmission line having the same cross-section as the port. In this analysis, the width of the wave ports was defined to be narrow enough so that only one mode was supported.
6. The full electromagnetic field pattern inside the structure (inside the problem area) is computed for the supported mode.
7. The *S*-matrix is computed based on the reflection and transmission that occurs.

8. The mesh is refined based on user settings, and steps 4-7 are repeated once more.

9. The two *S*-parameter solutions are used to estimate the regions of the problem domain where the solution has strong error by calculating the change in the magnitude of the S-parameters from the two passes. The magnitude and phase of all S-parameters are compared to the user's setting of Maximum Delta S Per Pass to determine if further mesh refinement is necessary.

10. If the *S*-Parameters change by an amount less than the Maximum Delta S Per Pass value from one iteration to the next, the adaptive analysis stops. Otherwise, the mesh is refined in the areas of strong error and the process is continued (find solution, calculate error, refine mesh) until the delta S criteria is met or the requested number of passes is completed.

11. The final mesh from the adaptive process is used to solve the problem at other frequencies based on the frequency sweep defined.

The values for the settings used in the analysis for this research are shown in Table 5.1 and are briefly described below:

- Solution Frequency: The frequency at which the adaptive process occurs

- Lambda Refinement: The initial mesh is refined so that each element has no edge longer than a fraction of a wavelength at the Solution Frequency. The Lambda Refinement parameter is this fraction.

- Port Field Accuracy: When solving for the fields (modes) on each port, this parameter defines the accuracy required before the next step in the adaptive process can occur.

- Maximum Number of Passes: Determines how many times the adaptive mesh refinement and solution generation process occurs if the solution convergence condition has not been met.

- Maximum Delta S Per Pass: The stopping criterion for the adaptive passes. It is the change in the magnitude of the *S*-parameters between two consecutive passes, and hence defines the convergence of the *S*-Parameters as the mesh is refined.

- Percent of Tetrahedra Refined Per Pass: If the mesh needs to be refined, this parameter defines how much refinement will occur in terms of the number of elements that will be added (expressed as a percentage).

Table 5.1. HFSS solution parameters used for all simulations.

Parameter	Value
Solution Frequency	40 GHz
Lambda Refinement	0.0333
Port Field Accuracy	0.01
Maximum Delta S Per Pass	0.01
Percent Refinement Per Pass	20 %
Maximum Number of Passes	5

5.7. Description of Output Data

HFSS provides many means of viewing the solution data. The electric fields and currents can be viewed and animated. All of the data from the adaptive process is saved for review, including the number of tetrahedra, the solution time, and the convergence data for each adaptive pass. For this work, only the *S*-parameters were needed, so they were exported to a data file for plotting. By exporting the data to a file, it could then be compared to data from the analytical modeling and testing in plots. All results are shown in Chapter 7.

5.8. Summary

Ansoft HFSS, the software tool that was used to simulate the RF performance of the encapsulation designs, was introduced in this chapter. The chapter included a description of how to use HFSS, how the software performs finite element analysis, and the specific settings that were used in this work. The next chapter presents the test equipment and procedures that were used to obtain experimental data from the unencapsulated RF MEMS switch, and the RF MEMS switch with a dielectric encapsulation. All data is presented and compared in Chapter 7.

5.9. References

[1] Ansoft High Frequency Structure Simulator (HFSS), version 9.0, Ansoft Corporation, 2003.

[2] Muldavin, J. B. and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches—part I: modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp.1045-1052, Jun. 2000.

[3] Wong, C. H., M. J. Tan, and K. M. Liew, "Electrical characterization of RF capacitive microswitch," *Sensors and Actuators A: Physical*, vol. 102, pp. 296-310, Jan. 2003.

6. Laboratory Testing of RF MEMS Switches

The AFRL capacitive switches with and without dielectric encapsulations were fabricated and tested by engineers at the Air Force Research Laboratory, Sensors Directorate, (AFRL/SN) at Wright-Patterson Air Force Base. This test data was used for comparison to the analytical model data and the full-wave electromagnetic simulation data. The test equipment and procedures are described below.

6.1. Instrumentation Configuration

The RF MEMS switches (unencapsulated and encapsulated) that were fabricated were made on 3 inch diameter sapphire wafers, and did not undergo any subdivision or further packaging. Therefore, all measurements had to be taken on-wafer. One advantage of RF components based on CPW transmission lines is the simplicity of on-wafer measurements using RF micro-probes known as GSG (Ground-Signal-Ground) probes. The GSG probe allows for the testing of CPW-based devices with only two probes (each consisting of three points), one at each end of the CPW. Figure 6.1 shows a drawing of two GSG microprobes positioned on a RF MEMS switch. The GSG probes are attached to high precision micropositioners for precise placement, and placement is accomplished with the aid of a microscope.

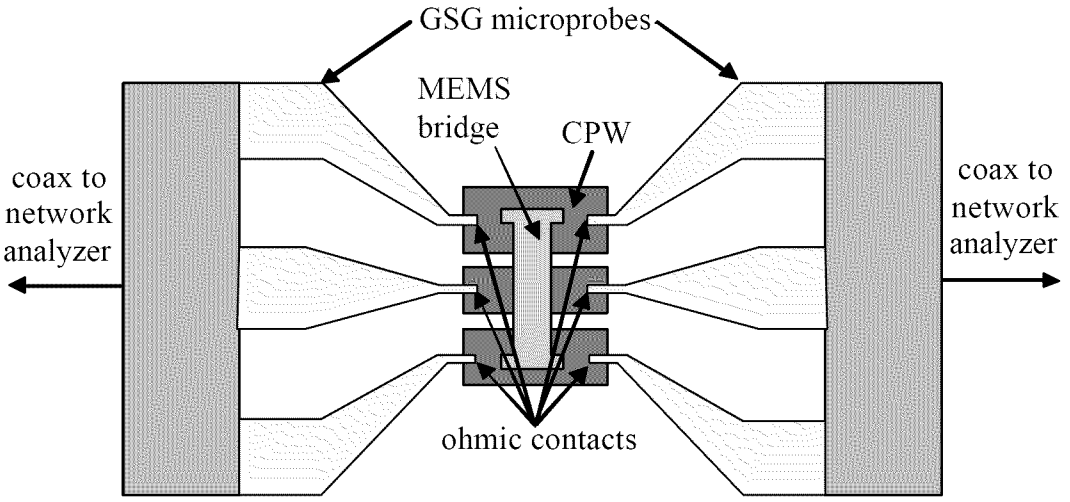


Figure 6.1. Drawing of a CPW-based MEMS switch with GSG (Ground-Signal-Ground) microprobes for on-wafer RF testing.

A block diagram of the instrumentation setup is shown in Figure 6.2. An HP 8510C vector network analyzer with an HP 8517 S-parameter test set was used to extract the *S*-Parameters from the device. The frequency sweep used went from 1-26 GHz at 0.5 GHz increments. Data was not taken at higher frequencies due to the limitations of the bias tees. The network analyzer was configured to perform 64 point data averaging in step mode. In step mode, the network analyzer collects all of the data samples at one frequency, then steps to the next frequency and collects 64 data points at that frequency, and so forth. For the switch to be tested in the down position, a DC bias between the ground and signal lines of the CPW was required. Bias tees were inserted between the ends of the network analyzer leads and the three-point probes to introduce the DC bias signal onto the RF signal line of the device under test (DUT). The bias tee provides the DC bias to the DUT while preventing the DC bias signal from propagating into the network analyzer and preventing the RF signal from propagating into the bias network. The bias network consisted of an Agilent 33250A frequency/waveform generator connected to an Av-

tech AV-112A high-voltage amplifier. The bias voltage signal was a 1 kHz bipolar square wave with a duty cycle of 100%. The DC bias is signaled this way to prevent the RF dielectric from becoming electrically charged, which would cause performance instability of the RF MEMS switch. The magnitude of the voltage required to hold the switches in the down position was roughly 30 V.

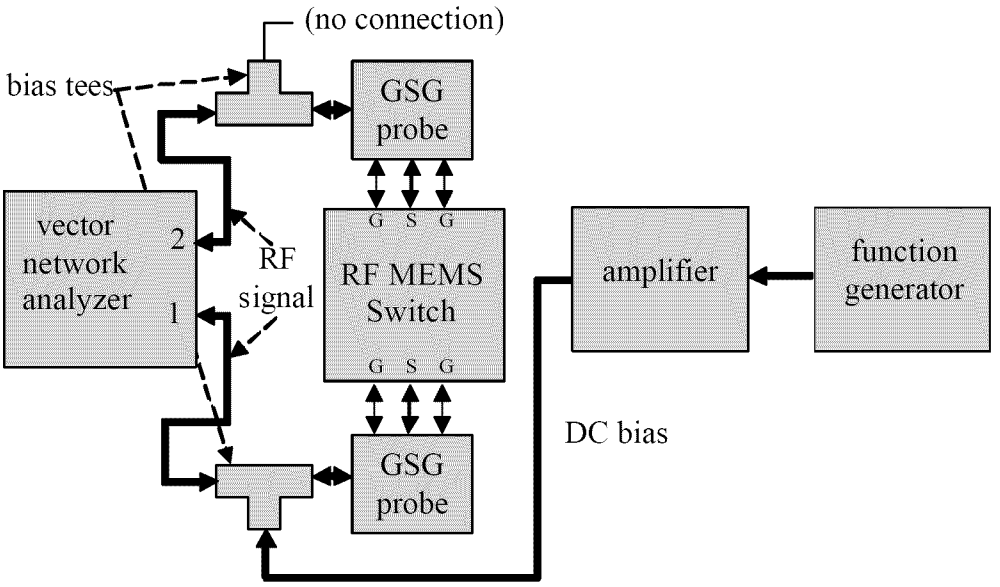


Figure 6.2. Block diagram of the instrumentation setup for *S*-parameter measurement of the RF MEMS devices in the AFRL cleanroom. The thick lines represent coaxial cable, where the thin lines represent regular leads or connections.

A photograph of the instrumentation setup in the laboratory is shown in Figure 6.3. Here the probe station is shown as the center of the test setup. The probe station holds the micro-probes under the microscope on a vibration-controlled stand. Connected to the micro-probes are the bias tees which pass through the RF signal from the network analyzer behind the probe station and add the DC bias signal from DC bias network to the left of the probe station.

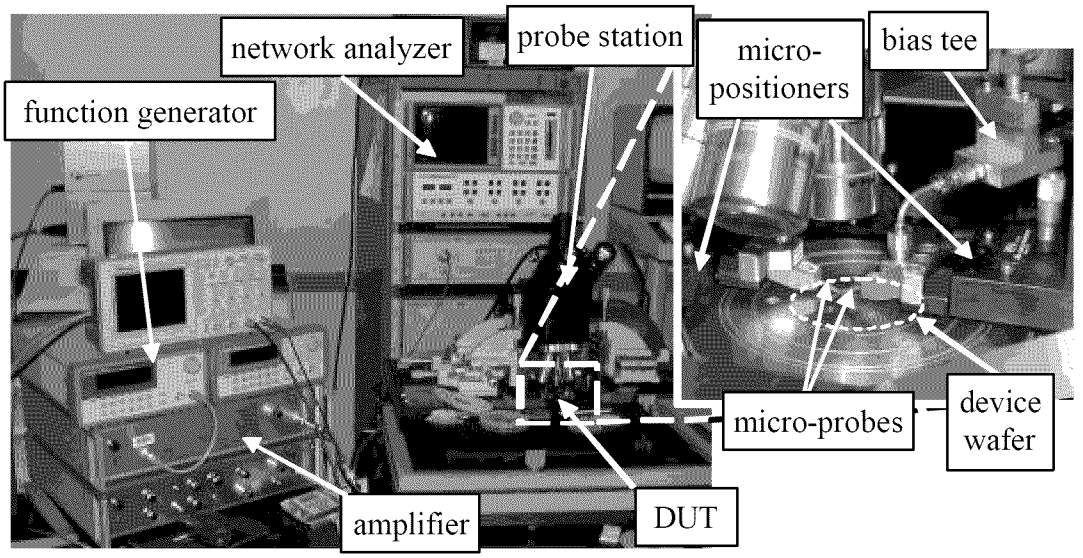


Figure 6.3. Picture of the RF MEMS test setup in the AFRL cleanroom used to extract the *S*-paramters from RF MEMS switches. A blow-up view of the device wafer with the micro-probes positioned on it is also shown.

6.2. Calibration and Testing Procedure

The network analyzer was calibrated to the ends of the probe tips using the standard SOLT (short, open, load, through) calibration procedure. This calibration involves one-port short, open, and load measurements on a standard, for each port. Then a two-port measurement of a through (a length of transmission line) is taken. An impedance standard substrate (ISS) from Cascade Microtech was used as the calibration standard. After calibration, the probes were put on the DUT and data was taken. The probes were aligned on the CPW of the DUT so that the reference planes were approximately 100 μm from the ends of the CPW lines. The data from the measurements was saved to a data file for later plotting and comparison. All results from testing are presented and discussed in Chapter 7.

6.3. Discussion of Data Accuracy

Because RF MEMS are inherently low loss, high isolation devices, even small errors or inaccuracies introduced into the measurement will have a significant effect on the measured performance of the devices. Multiple potential sources of error exist for the *S*-parameter data used in this research. First, the calibration is performed using an ISS, a very high performance RF standard. One source of measurement error that is calibrated out in the calibration process is contact resistance between the probes and the CPW. The difference in the contact resistance between the calibration standard and the device wafer is a source of error. This is sometimes handled by fabricating the calibration standards directly on the device wafer, which negates any potential error in calibration due to contact resistance.

Another source of error is sensor drift of the network analyzer. Each device was tested at different times by the network analyzer, with up to several minutes elapsing between measurements. This time can lead to the analyzer "drifting" out of calibration due to a temperature change within the instrument. Because of this drift, less confidence can be given to the data when comparing different measurements to each other.

6.4. Summary

The equipment and procedures that were used by AFRL to obtain experimental data from an uncapsulated RF MEMS switch and one with a dielectric encapsulation were described in this chapter. The key instrument in extracting the S-parameters from the devices was a network analyzer, and possible sources of error from that instrument were discussed. The next chapter presents the test data and compares it to the modeling and simulation data also obtained on the devices.

7. Results, Proposed Designs, and Proposed Fabrication Process

In this chapter, all results from analytical modeling, full-wave electromagnetic simulation, and laboratory experimentation will be presented, compared, and discussed. The computer code that was used to produce these data plots is presented in Appendix E. The results are used to design an optimized encapsulation, which is described in Chapter 8. The results from analysis of metal reflow over an etch hole are also presented in this chapter.

7.1. Analytical Model Results

Using the lumped-element equivalent circuit analytical models developed in Chapter 4 for the switch and encapsulation designs described in Chapter 3, the *S*-parameters were extracted using Ansoft Designer SV [1], a high frequency circuit analyzer software program. For comparison, the insertion loss data is shown in Figure 7.1, the return loss data is presented in Figure 7.2, and the isolation data is shown in Figure 7.3. The model data is compared to test and simulation data and discussed in detail in Sections 7.3-7.6.

Figure 7.1 shows that the switch with no encapsulation has the lowest insertion loss, as expected. All designs that have the metal layer confined to the top of the encapsulation (3,4,7-9) have roughly the same insertion losses. The unencapsulated switch has an insertion loss of about -0.2 dB at 40 GHz, while the worst performing encapsulation design (4) has an insertion loss of about -0.32 dB at 40 GHz. Designs 5 and 6 have considerably greater losses than any of the other design, with design 5 having an insertion loss of -1.15 dB at 40 GHz. This data shows that in terms of insertion losses, all of the designs

except 5 and 6 have reasonable insertion loss performance as compared to the unencapsulated switch.

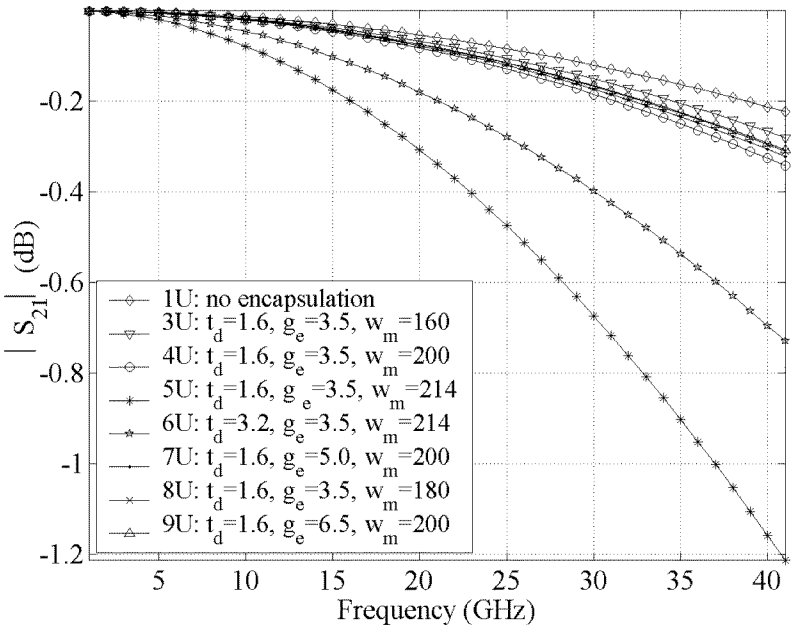


Figure 7.1. Plot showing all insertion loss results from analytical modeling of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

Figure 7.2 shows a plot of the analytically modeled return loss data from all designs. Again we see that all designs except designs 5 and 6 have about the same return loss performance as the unencapsulated switch. This is because designs 5 and 6 present a much different impedence mismatch than the other designs due to designs 5 and 6 having part of the metal layer so much closer to the signal line than the other designs. This impedence mismatch causes the higher values of return loss for designs 5 and 6.

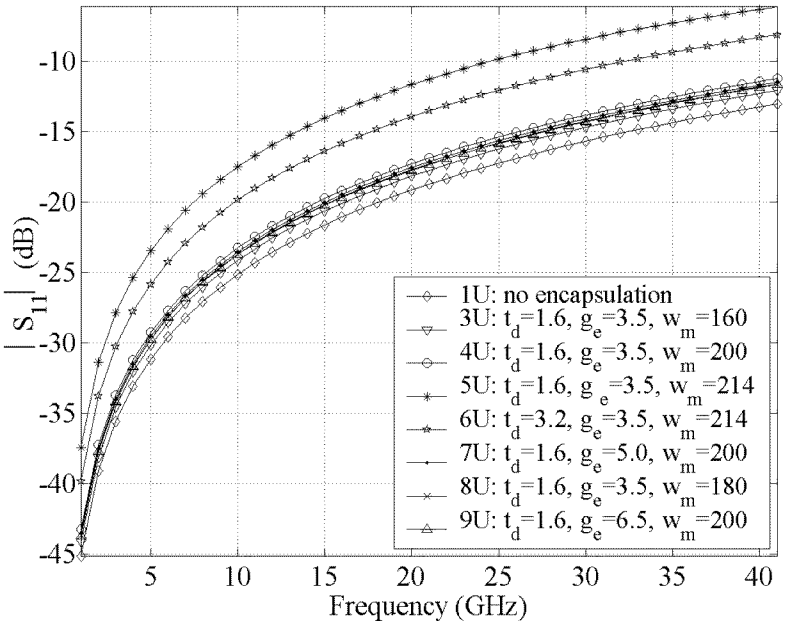


Figure 7.2. Plot showing all return loss results from analytical modeling of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

Figure 7.3 shows a plot of the analytically modeled isolation data for all encapsulation designs. In this plot we see that all designs have about the same isolation performance. The designs with metal layers actually have better isolation than the unencapsulated switch and the dielectric encapsulated switch due to the added coupling to the encapsulation. This is expected because for maximum isolation, it is desired to have the strongest coupling possible from signal to ground.

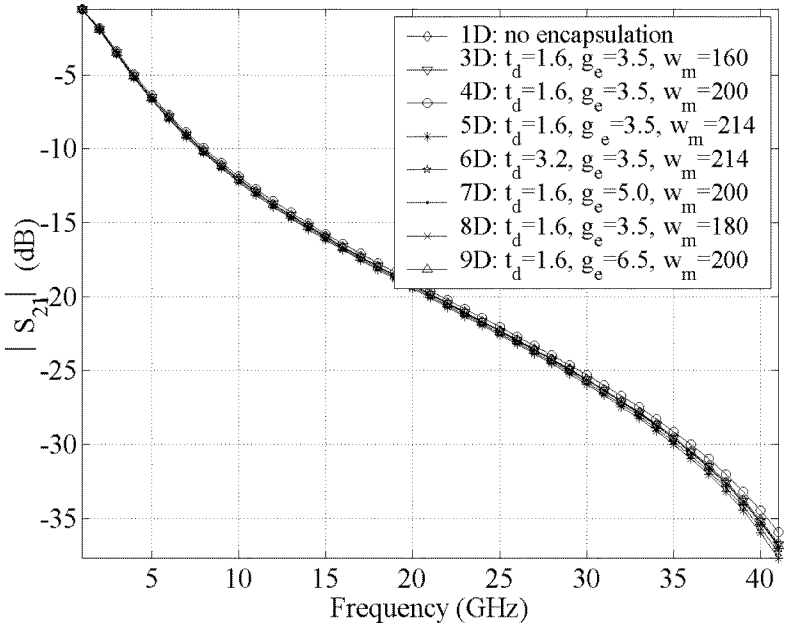


Figure 7.3. Plot showing all isolation results from analytical modeling of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

7.2. Full-Wave Electromagnetic Simulation Results

Using the solid models of the designs and simulation parameters as described in Chapter 5, HFSS [2] simulations were run on each design. The insertion loss, return loss, and isolation data are presented in Figures 7.4-7.6. The data is also presented and discussed in detail in Sections 7.3-7.6 where it is compared with analytical model and test data.

Figure 7.4 shows a plot of the HFSS simulated insertion loss data for all designs. The performance is similar to the analytically modeled data, and the data sets will be compared and discussed in Sections 7.3-7.6.

Figure 7.5 shows a plot of the HFSS simulated return loss data for all designs. Again, the relative performance of the designs is similar to the analytically modeled data, and the data sets will be compared and discussed in Sections 7.3-7.6.

Figure 7.6 presents HFSS simulated data for the isolation performance of all designs. Again we see that there is not much difference between the designs in terms of isolation performance, and the encapsulations with a metal layer have slightly better isolation than those that do not.

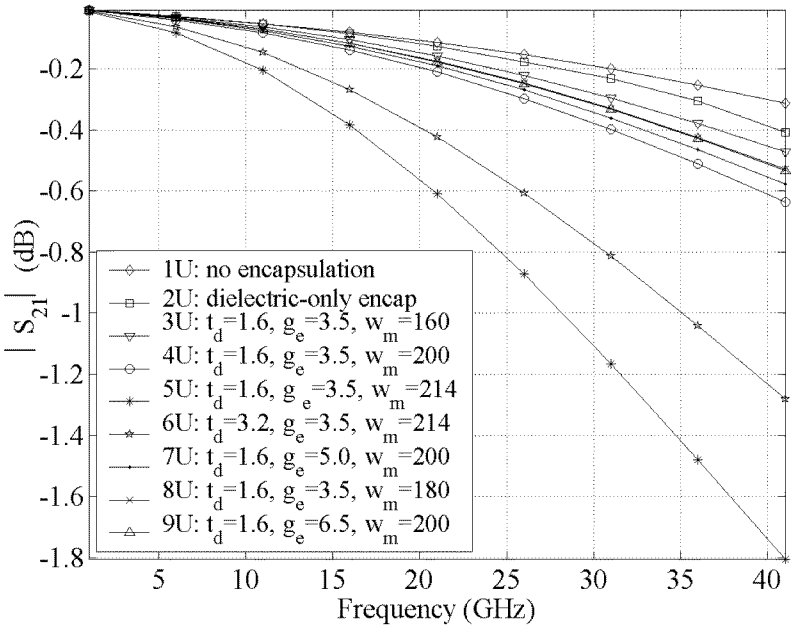


Figure 7.4. Plot showing all insertion loss results from HFSS simulation of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

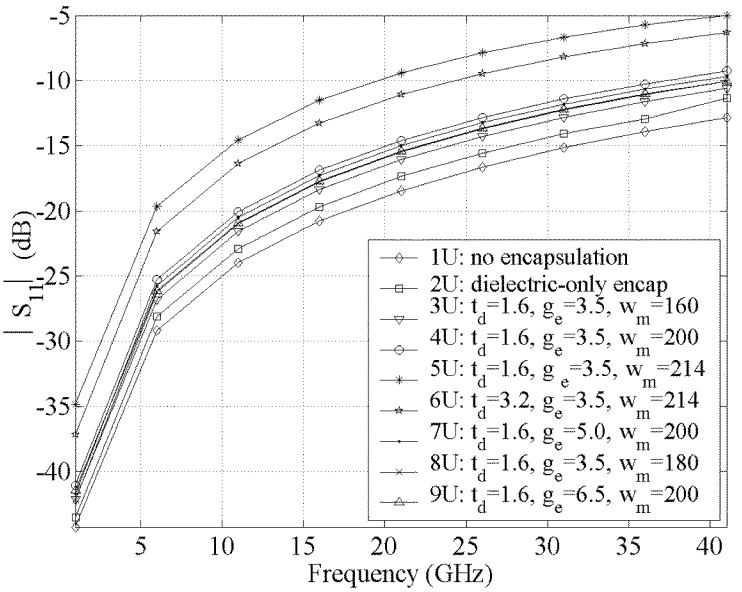


Figure 7.5. Plot showing all return loss results from HFSS simulation of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

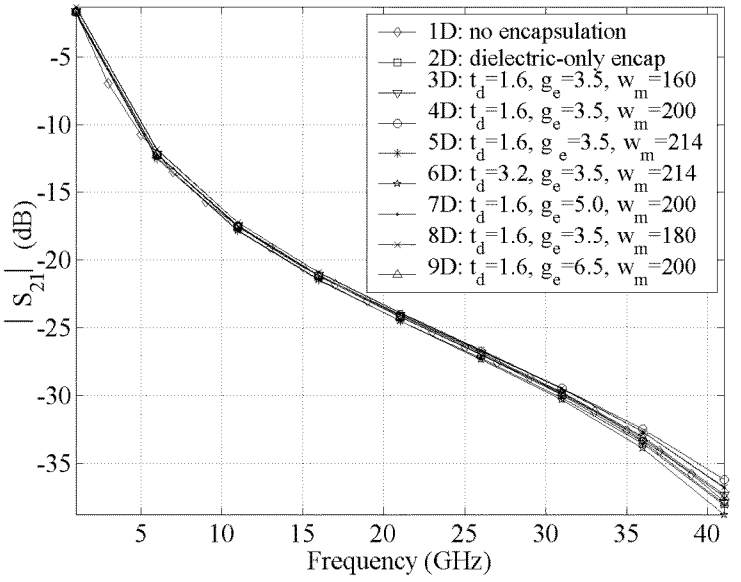


Figure 7.6. Plot showing all isolation results from HFSS simulation of the RF MEMS switch, with and without an encapsulation. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the key geometry values for that design. All dimensions are given in μm.

7.3. Experimental Results and Comparison to Model and Simulation Results

The insertion loss test data for the switch in the up position with and without a dielectric encapsulation is shown in Figure 7.7. Also shown in the figure are the results from analytical modeling and full-wave simulations for comparison and assessment of their accuracy.

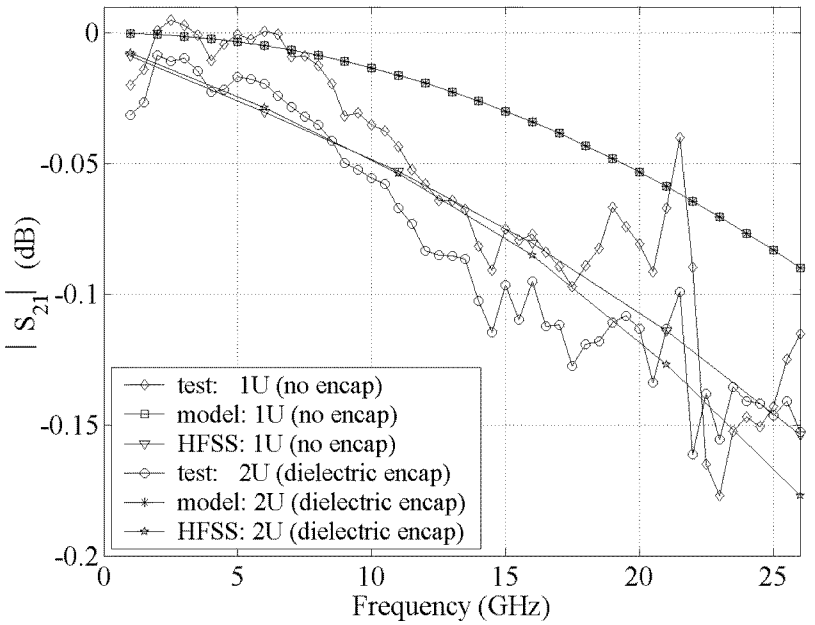


Figure 7.7. Plot comparing insertion loss results from device testing, analytical modeling, and HFSS simulation of the unencapsulated and dielectric encapsulated switches. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the encapsulation details for that design.

Although the test data is somewhat noisy, a general trend can easily be seen from the data. Clearly, as frequency increases the insertion loss also increases (becomes more negative in dB) for both the encapsulated switch and the unencapsulated switch. This is expected because at higher frequencies the capacitive coupling between the CPW signal line and the MEMS bridge becomes stronger. In addition, a slight but consistent increase

in insertion loss can be seen when the dielectric encapsulation is added. The added loss on average is about 0.02 dB. This loss is very small, and could very well be attributed to measurement or calibration error. However, it is expected that the dielectric encapsulation will cause a small loss in the switch. This is because the dielectric is not ideal, and it allows a very small amount of conduction current to flow through it, from signal to ground, resulting in signal loss.

The analytical model does not account for lossy dielectrics, so the data sets for the encapsulated switch and dielectric encapsulated switches are identical. Because the difference between the two cases is very slight in reality (as shown by the test data), it is not a poor approximation to use the unencapsulated model data for the dielectric encapsulated switch also. The model follows the same trend of insertion loss as the test data, but underestimates the insertion loss by about 0.03 dB at 10 GHz and 0.06 dB at 26 GHz. The underestimation of insertion loss by the analytical model is also seen when comparing it to the simulation data for every design in this research. Listed below are some possible reasons why the model might underestimate the insertion loss of the switch:

- The fringing field capacitance may have been underestimated, or oversimplified in the model.
- The actual geometry and material parameters of the tested devices may be slightly different than the values used in the models.
- The model assumes every layer is planar and perfectly flat, and does not account for the conformality of each layer due to the fabrication process. Also, any bending of the beam due to compressive residual stress that may exist in the actual device is not known or accounted for. These factors may contribute to an underestimation of the capacitance.

The data from HFSS simulation is also shown in Figure 7.7. The simulation data follows the trend of the test data relatively well, and shows a very slight increase in inser-

tion loss with the addition of the dielectric encapsulation. The increase in insertion loss due to the dielectric encapsulation is smaller than the test data shows, especially at lower frequencies, which could be due to using a value for the dielectric loss (loss tangent, tan d_d) in HFSS that was too small.

The return loss test data for the switch in the up position with and without a dielectric encapsulation is shown in Figure 7.8. Again, the results from analytical modeling and full-wave simulations are also shown for comparison and assessment of their accuracy. A slight increase in insertion loss is seen with the addition of the dielectric encapsulation. This is also seen in the simulation data. The overall data trends of the model, simulation, and test data are similar, although the model and simulation underestimate the return losses. This could also be caused by inaccuracies in calculating the capacitance value in the model or in inaccuracies of the material parameters or geometry in the simulation. The crossover of the HFSS data with the modeled data at 5 GHz is only due to the resolution of the HFSS data. If the same designs were simulated at more frequencies below 6 GHz, the HFSS data trace would probably not cross over the modeled data trace.

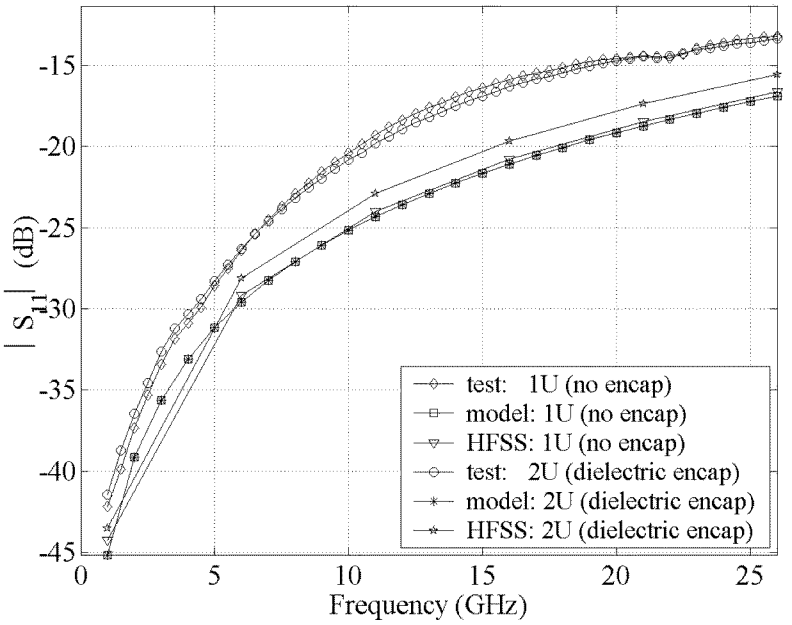


Figure 7.8. Plot comparing return loss results from device testing, analytical modeling, and HFSS simulation of the unencapsulated and dielectric encapsulated switches. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the encapsulation details for that design.

The isolation test data for the switch in the down position with and without a dielectric encapsulation is shown in Figure 7.9. Again, the results from analytical modeling and simulations are also shown for comparison and assessment of their accuracy. The test data shows a very small but measurable increase in isolation (more negative in dB) with the addition of the dielectric encapsulation. The analytical model and HFSS simulation both follow the trend of the test data, with the model being more accurate than the simulation with respect to the test data. The reason for the overestimation of the insertion loss in the simulation is that the surface roughness of the RF dielectric is not accounted for in the simulation, which leads to stronger electromagnetic coupling between the MEMS bridge in the down state and the signal line, resulting in higher isolation. Because of this,

the analytical model more accurately calculates isolation than the simulation with respect to the test data.

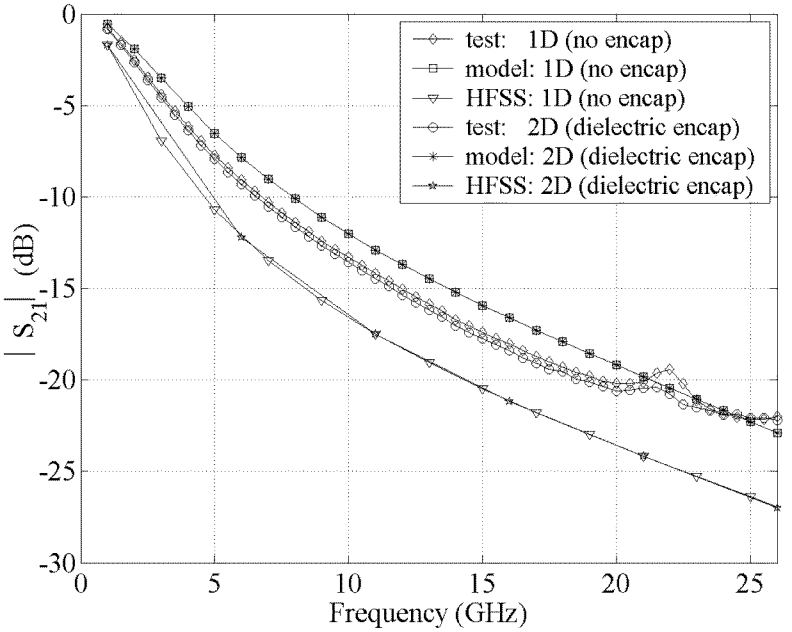


Figure 7.9. Plot comparing isolation results from device testing, analytical modeling, and HFSS simulation of the unencapsulated and dielectric encapsulated switches. For the convenience of the reader, each data trace in the legend is labeled with both the design configuration number it represents along with the encapsulation details for that design.

In this research, insertion loss is generally a more important metric to optimize than isolation. In general, the isolation of the switch will only be improved by the addition of an encapsulation with a metal layer due to the additional coupling of the signal from signal to ground. In RF packaging, minimization of insertion loss is generally more important than maximizing isolation. Therefore, because the HFSS results more closely follow the test data for insertion loss, it was relied on more heavily in comparison of the performances of the designs and in designing the optimized encapsulation. In addition, because the simulation is based on rigorous electromagnetic theory with very few simpli-

fying assumptions, it is assumed to be more accurate than the analytical model. The analytical model was accurate enough to use as a "sanity check" for the test data and the HFSS simulation data.

7.4. Effect of Varying the Metal Layer Width, w_m

One of the design variables for the metal layer of the encapsulation was its width, w_m. In Figure 7.10 the analytical model and HFSS simulated insertion losses of three different widths are shown. In all three designs, the metal layer rests completely on the top of the encapsulation; it does not extend down the sides of the dielectric encapsulation. For all three widths, the dielectric encapsulation width (w_d) is 200 µm and the encapsulation height (g_e) is 3.5 µm. Both the model and simulation show an increase in insertion loss as the metal width is increased. The simulation data is assessed to be more accurate, as described Section 7.3. The results show that to minimize the insertion loss due to the encapsulation, the metal layer width should be as small as possible. A necessary constraint for the width of the metal layer is that it must be wide enough to encompass all of the etch holes in the dielectric encapsulation. Also, some engineering tradeoffs exist in minimizing the metal layer. For example, the metal layer must be wide enough to cover all of the etch holes, and a narrower metal layer will not give the encapsulation as much mechanical strength or electromagnetic shielding as a wider metal layer. Electrical shielding and mechanical strength of the encapsulation are not assessed in this research. Etch holes in the dielectric layer are spaced no more than 40 µm apart, so the metal layer must be at least 160 µm wide in order for the etch holes nearest the sides of the encapsulation to be covered by the metal layer. Therefore, in order to minimize the insertion loss due to

the encapsulation, but still have it large enough to cover all of the etch holes during reflow, a metal layer width of 160 μm is chosen.

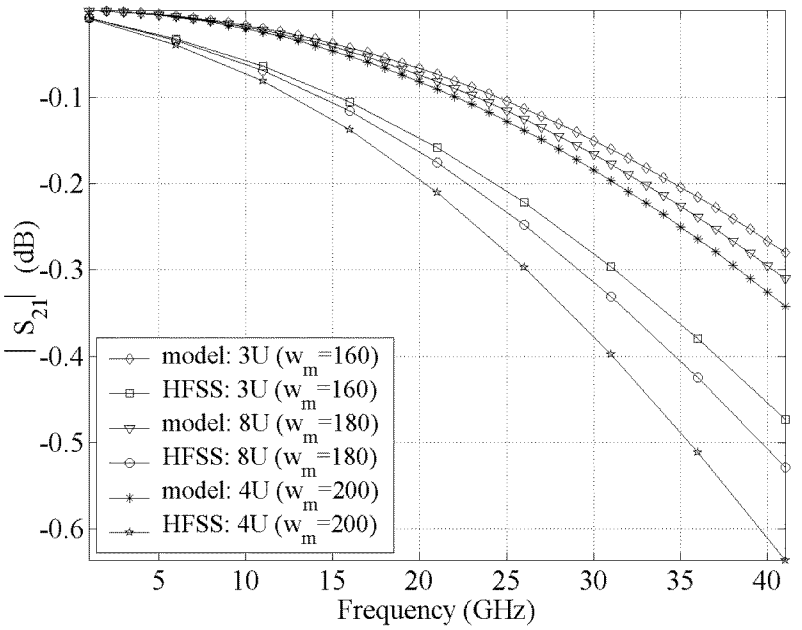


Figure 7.10. Plot comparing the insertion loss results from analytical modeling and HFSS simulation of encapsulation designs where only the metal layer width, w_m, was varied. For the convenience of the reader, all data traces in the legend are described with both the design configuration they represent along with the key dimension of the metal encapsulation layer that was varied. In all designs, w_d=200 μm, t_d=1.6 μm, and g_e=3.5 μm. All dimensions are given in μm.

7.5. Effect of Varying the Encapsulation Sacrificial Layer Thickness, g_e

Another design variable that was varied was the thickness of the encapsulation sacrificial layer. This thickness could also be referred to as the air gap between the MEMS beam and the encapsulation, g_e. In Figure 7.11 the analytical model and simulation results for insertion loss with three different encapsulation heights are shown. Both the analytical model and simulation show that as the encapsulation height is increased, the insertion loss decreases. The maximum encapsulation height will be dictated by the limits of the fabrication process used to create the encapsulation. According to AFRL, the

desired maximum encapsulation height is 3.5 μm, with a hard limit of 6.5 μm. Based on the data, it is desired to increase the encapsulation height to 5.0 μm.

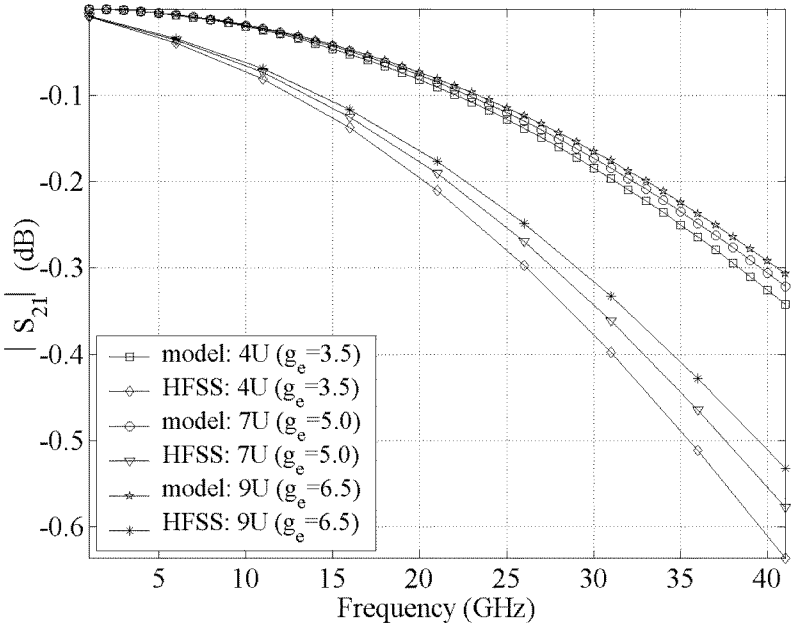


Figure 7.11. Plot comparing the insertion loss results from analytical modeling and HFSS simulation of encapsulation designs where only the encapsulation sacrificial layer height, g_e, was varied. For the convenience of the reader, all data traces in the legend are described with both the design configuration they represent along with the key dimension of the encapsulation that was varied. In all designs, w_d=200 μm, w_m=200 μm, and t_d=1.6 μm. All dimensions are given in μm.

7.6. Effect of Varying the Dielectric Layer Thickness, t_d

The third design variable that was varied was the thickness of the encapsulation dielectric layer. This was performed as an attempt to improve the insertion loss of the design where the encapsulation metal layer was 214 μm wide, which was poor. In this design, the encapsulation metal layer was wider than the dielectric layer (w_m>w_d), so the metal layer conformed down the sides of the encapsulation and was separated from the signal line only by the width of the dielectric layer. In Figure 7.12 the analytical model

and simulation results for insertion loss with the two different dielectric layer thicknesses is shown. Both the analytical model and simulation show that as the thickness is increased, the insertion loss decreases. However, the performance is still poor, and would continue to be poor even if the dielectric thickness was increased to the maximum feasible thickness for fabrication. Based on the data, these designs were eliminated from consideration. For the designs where the metal layer width is less than the dielectric layer width, the dielectric thickness increase will contribute to slightly better insertion loss. It is simple to fabricate the dielectric layer to be 3.2 μm thick to gain this performance, so this thickness will be used in the final design.

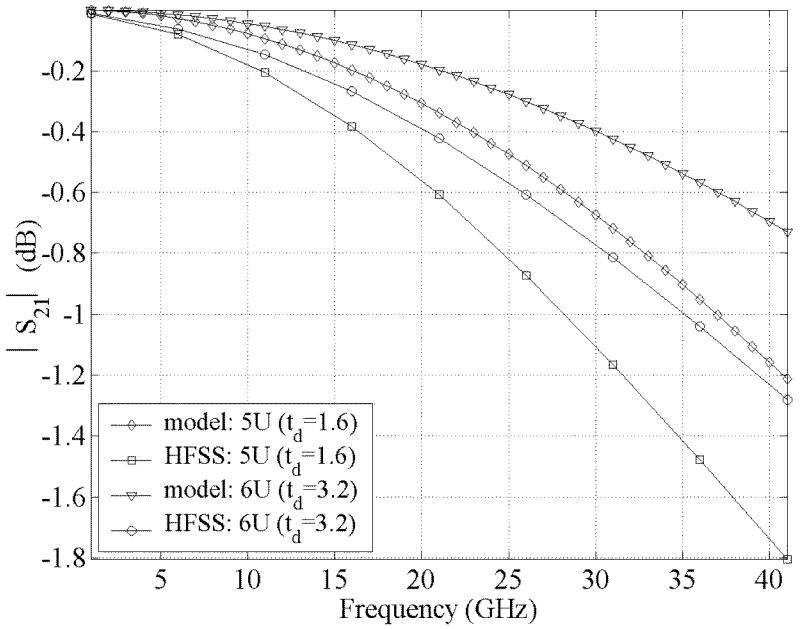


Figure 7.12. Plot comparing the insertion loss results from analytical modeling and HFSS simulation of encapsulation designs where only encapsulation dielectric layer thickness, t_d, was varied. In all designs, w_d=200 μm, w_m=214 μm, and g_e=3.5 μm. For the convenience of the reader, all data traces in the legend are described with both the design configuration they represent along with the key dimension of the encapsulation that was varied. All dimensions are given in μm.

7.7. RF Feed-Through Results

In the previous section, it was shown that the designs where the metal layer conforms down the sides of the dielectric encapsulation and onto the dielectric pad around the encapsulation had very poor insertion loss performance. In addition, the closeness of the metal encapsulation to the signal line also contributes to poor return loss. Using the theory shown in Chapter 4, the CPW was modified at the RF feed-through to provide for better performance. The return loss performance of the straight feed-through (the worst-case scenario) and the engineered RF feed-through are shown in Figure 7.13 for both the analytical model and HFSS simulation. The analytical model shows an improvement in return loss of about 2-3 dB, showing that the case of the straight RF feed-through can be improved with impedance matching techniques. More improvement was expected than what was given, and this performance could probably be improved with trial-and-error, or by applying the impedance matching theory differently. However, the improvement shown in the analytical model could not be replicated in the HFSS simulation, which showed almost no return loss improvement for the impedance matched design.

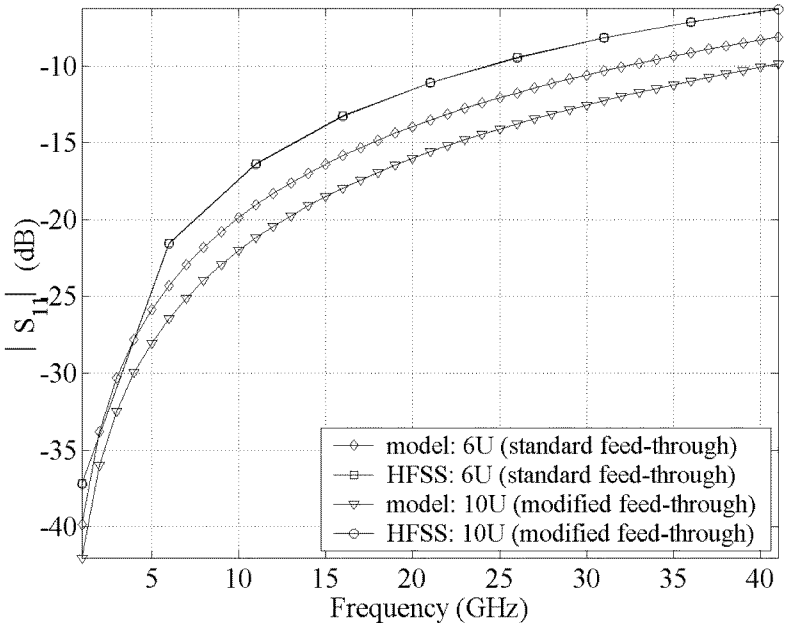


Figure 7.13. Plot comparing the return loss results from analytical modeling and HFSS simulation of the modified RF feed-through vs. the standard (straight; not impedance matched) feed through. For the convenience of the reader, all data traces in the legend are described with both the design configuration number they represent along with type of RF feed-through. In both designs, w_d=200 μm, w_m=214 μm, t_d=3.2 μm, and g_e=3.5 μm. All dimensions are given in μm.

It is expected that the RF feed-through modification will also have an effect on the insertion loss, and those results are shown in Figure 7.14. The analytical model shows a significant improvement in insertion loss (~0.26 dB at 40 GHz) with the impedance matched feed-through. This is due to the capacitance at the feed-through being smaller due to the narrower CPW signal line at that point. Again, the HFSS simulation results show little to no improvement in insertion loss for the impedance matched feed-through.

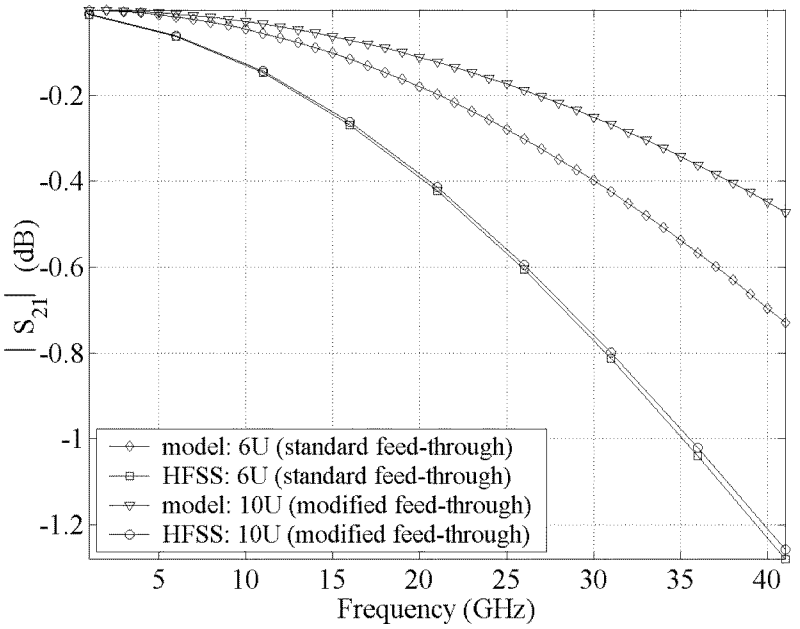


Figure 7.14. Plot comparing the insertion loss results from analytical modeling and HFSS simulation of the modified RF feed-through vs. the standard (straight; not impedance matched) feed through. For the convenience of the reader, all data traces in the legend are described with both the design configuration number they represent along with type of RF feed-through. In both designs, w_d=200 μm, w_m=214 μm, t_d=3.2 μm, and g_e=3.5 μm. All dimensions are given in μm.

Some possible reasons for the analytical model and HFSS simulation data not concurring are described below:

- The problem may have been oversimplified. The design was based on theory in the literature of impedance matching to a simple air bridge over a CPW. The actual geometry involves two connected air bridges, connected by a large air bridge at a different height between them, with another air bridge in the middle at a separate height. Possibly this theory cannot be used because it did not account for the many complex electromagnetic interactions that take place between all of the parts. Also, perhaps the transition should be impedance matched to the entire switch and encapsulation, not just the feed-through.

- The HFSS simulation may have been set up incorrectly. In all other designs, the encapsulation was the part of the geometry that was varied. In this design the CPW was modified, so it may have needed a smaller mesh size in order for the performance difference to be reflected in the results.

7.8. Results of Metal Reflow Modeling

The critical thickness of the metal layer is the thickness the metal layer must meet or exceed to guarantee hole closure on reflow for a given etch hole width. To solve for the critical thickness, multiple Surface Evolver runs were completed with the hole width fixed and the solder thickness varied. Figure 7.15 shows the graphical results from Surface Evolver of an etch hole width of 5 μm and a solder thickness of 5 μm. Clearly this is less than the thickness required to guarantee etch hole closing on reflow. In Figure 7.16, the result for a solder thickness of 6 μm is shown. In this case, the solder is thick enough for the hole to close on reflow.

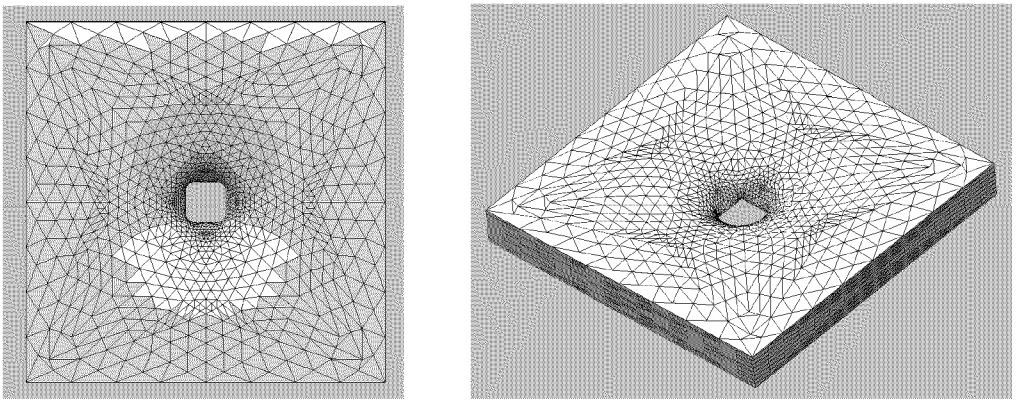


Figure 7.15. Surface Evolver graphical output showing the results after evolving the surface with a solder thickness, t_m, of 5.0 μm and a etch hole width, w_{eh}, of 5.0 μm.

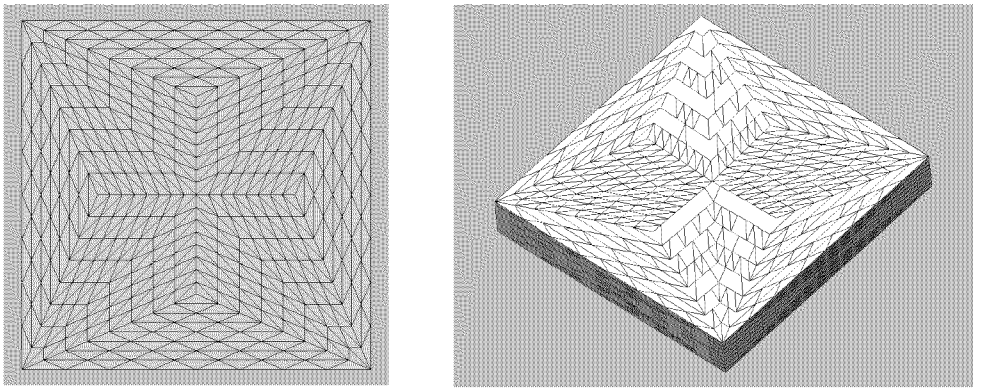


Figure 7.16. Surface Evolver graphical output showing the results after evolving the surface with a solder thickness, t_m, of 6.0 μm and an etch hole width, w_{eh}, of 5.0 μm.

For given hole widths, the thickness of the metal layer was interactively modified and analyzed in an iterative process to more precisely determine critical thickness of the metal layer. This analysis was done for etch hole widths of 3 μm and 5 μm, and the results are shown in Table 7.1. Analysis showed that for a hole width of 5 μm the critical metal thickness was 5.17 μm, resulting in a critical metal thickness to hole width ratio (t_m/w_{eh}) of 1.034. Stated differently, given a solder thickness of 5 μm, the etch hole width can be no wider than 4.83 μm to guarantee hole closure on reflow. Similarly, the critical thickness for a 3 μm hole was determined to be 3.11 μm, resulting in a critical t_m/w_{eh} ratio of 1.037. Because the critical ratio is nearly the same for the 3 μm and 5 μm holes, this ratio can be used for other hole sizes or thicknesses that are desired by the designer.

Table 7.1. Surface Evolver results showing the necessary metal layer thickness (critical thickness) for a given etch hole width to guarantee etch hole closure when the metal is reflowed. The hole width and metal thickness are then computed as a ratio for comparison between the two cases.

Etch Hole Width, w_{eh}	Critical Metal Thickness, t_m	Critical Ratio, t_m/w_{eh}
3 μm	3.11 μm	1.037
5 μm	5.17 μm	1.034

7.9. Summary

In this chapter the RF performance data from testing, analytical modeling, and electromagnetic simulation were presented and discussed. It was found that for the best RF performance with an encapsulation with a metal layer, the layer must be as narrow as possible, the dielectric layer must be as thick as possible, and the air gap between the MEMS device and the encapsulation must be as large as possible. These results were used to design an optimized encapsulation, which is presented in the next chapter. Analytical modeling also showed that impedence matching techniques can be used to improve the RF performance of the feed-through of the CPW signal line into the encapsulation. Finally, the optimum ratio of metal thickness to etch hole width was determined through modeling. This optimum ratio is what is necessary to guarantee the etch holes will close when the metal is reflowed. The next chapter presents the design of the optimized encapsulation as well as fabrication process that can be used to fabricate it using standard thin film techniques.

8. Optimized Encapsulation Design and Fabrication Process

All of the modeling, simulation, and testing data was used to create an optimized encapsulation design and a fabrication process to fabricate the encapsulations. The encapsulation design and fabrication process are presented in this chapter.

8.1. Optimized Encapsulation Design

Based on the data from analytical modeling, electromagnetic simulation, and laboratory testing, in addition to the limits of the fabrication process, an optimized encapsulation has been designed. The geometry values for the encapsulation are shown in Table 8.1.

Table 8.1. Dimensions of the optimized encapsulation.

Variable	Symbol	Value (μm)
Sacrificial Layer Thickness	g_e	5.0
Dielectric Layer Width	w_d	200
Dielectric Layer Thickness	t_d	3.2
Metal Layer Width	w_m	160
Metal Layer Thickness	t_m	5.0
Etch Hole Diameter	w_{eh}	3.0

8.2. Proposed Thin Film Fabrication Process

A novel fabrication process, based on the AFRL process that was used to fabricate the switch and the dielectric encapsulation, is proposed below. In creating this process, the manufacturing capabilities of the AFRL clean room were taken into consideration [1].

The proposed fabrication process is different from the fabrication processes described in Chapter 2 in several ways. First, the proposed fabrication process uses standard thin film techniques and materials. The only post-process step is the very last step, which is the sealing of the etch holes. Most other techniques involve extensive post-processing.

Second, most existing packaging techniques use high-temperature (> 200°C) processes to fabricate the encapsulations that would be harmful to the MEMS device. The proposed fabrication process does not involve any high temperature processes. Finally, the proposed fabrication process employs a solder reflow step to seal the etch holes. No other known process uses a solder reflow step to seal etch holes.

The process starts with the unreleased AFRL switch fabricated as described in Section 2.2.2. The first step in the proposed encapsulation process is to deposit 5.0 μm of PMGI (e-beam resist) and pattern it with optical resist over the entire unreleased switch, as shown in Figure 8.1. The PMGI sacrificial layer "forms" are next reflowed at 250°C to create rounded sidewalls.

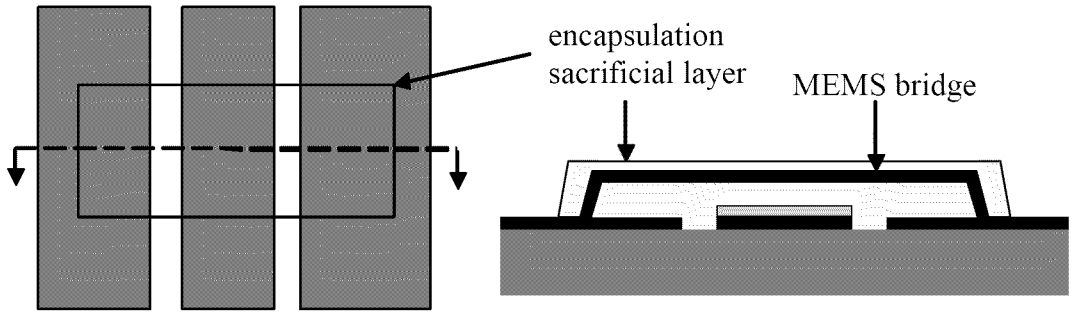


Figure 8.1. (a) Top view and (b) side cut-away drawings of the switch and encapsulation after the first step of the encapsulation fabrication process, where the sacrificial layer that defines the encapsulation has been deposited and patterned.

Next, 3.2 μm of silicon nitride is deposited by sputtering, as shown in Figure 8.2. This layer is patterned over the sacrificial layer to create an encapsulation over each switch using optical resist as the etch mask. Next, etch holes that are 3 μm in diameter are patterned in each encapsulation and etched with reactive ion etching (RIE) or wet chemical etching. These etch holes must not be spaced more than 40 μm apart from each other

to ensure sacrificial layer is completely etched away during the release step. In addition to the etch holes, voids are created in the silicon nitride layer over the CPW ground traces. These voids allow the metal layer to make electrical contact with the ground traces.

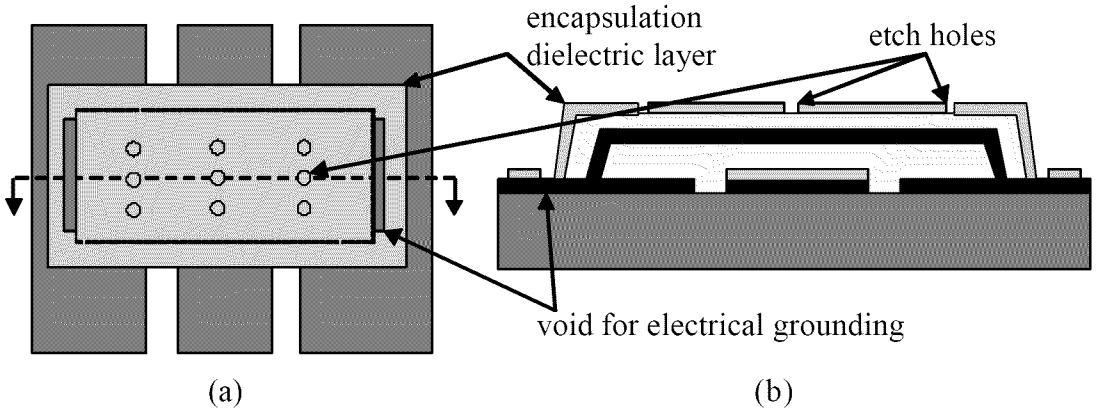


Figure 8.2. (a) Top view and (b) side cut-away drawings of the switch and encapsulation after the second step in the encapsulation fabrication process. Here the encapsulation dielectric layer has been deposited and patterned. Note the voids in the layer over the CPW ground planes so the metal layer, when deposited, will be electrically grounded. Also, etch holes are patterned so the device can be released. The etch hole size and quantity in the drawing is inaccurate but is shown this way for clarity to the reader.

Next, the metal layer of the encapsulation is defined by depositing a 7-10 μm thick layer of photoresist over the dielectric encapsulation and patterning it to create a "mold" for the metal layer, as shown in Figure 8.3. This encapsulation "mold" also defines 3 μm diameter etch holes over the existing etch holes in the dielectric layer. This will allow for release of the sacrificial layers because the etch holes in the dielectric layer and the metal layer will be aligned.

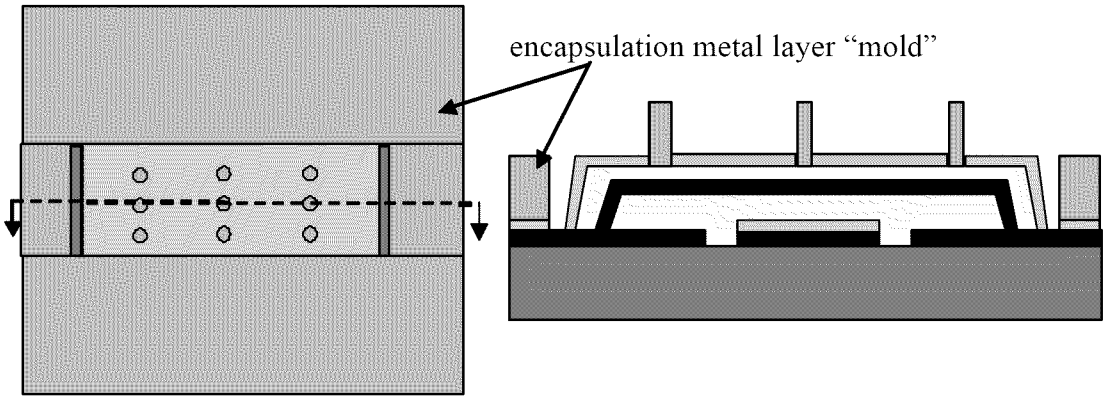


Figure 8.3. (a) Top view and (b) side cut-away drawings of the encapsulation after the third step in the encapsulation fabrication process. Here a 7-10 μm thick photoresist "mold" that defines the metal layer has been deposited and patterned. The places where the photoresist mold doesn't exist are the areas where the metal layer will exist when fabrication is complete.

Next, the metal layer, consisting of 5 μm of indium solder is sputtered over the wafer, as shown in Figure 8.4.

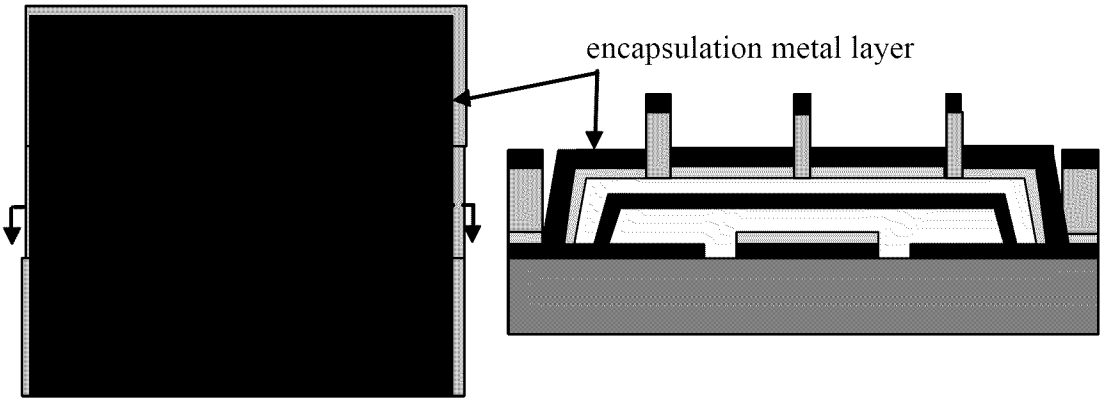


Figure 8.4. (a) Top view and (b) side cut-away drawings of the encapsulation after the fourth step in the encapsulation fabrication process. Here the metal layer of indium solder has been sputter deposited over the entire wafer. The mold created in the previous step will allow the undesired metal parts to be removed with the lift-off method.

In the next fabrication step, the undesirable parts of the metal layer are removed using the lift-off method and the remaining photoresist mold is removed using photoresist

stripper, as shown in Figure 8.5. Now a clear path to the sacrificial layers via the etch holes has been uncovered, allowing for the sacrificial layers to be removed in the next step.

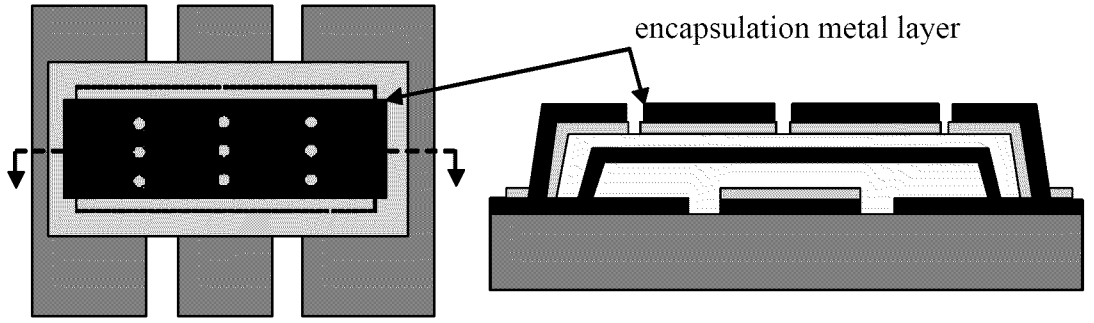


Figure 8.5. (a) Top view and (b) side cut-away drawings of the switch and encapsulation after the fifth step in the encapsulation fabrication process. Here the lift-off method has been used to remove the unwanted areas of the metal layer, and the photoresist mold has been stripped away.

Next, the sacrificial layers of PMGI that defined the suspended MEMS bridge and the encapsulation are released by soaking in PMGI stripper, as shown in Figure 8.6. Immediately following the release, the switches are dried using a CO_2 critical point drying process to prevent stiction.

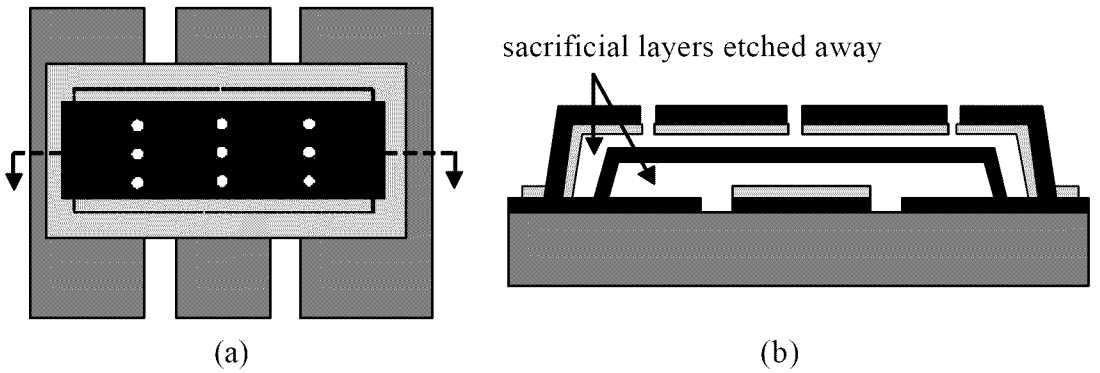


Figure 8.6. (a) Top view and (b) side cut-away drawings of the switch and encapsulation after the sixth step in the encapsulation fabrication process, showing that the RF MEMS switch and encapsulation have been released by etching away the sacrificial layers.

Finally, the etch holes are sealed by placing the wafer in a oven and raising the temperature above the melting point of indium solder, which is 156°C [2], as shown in Figure 8.7. The oven should be at ambient pressure of a dry, inert gas for optimum switch reliability.

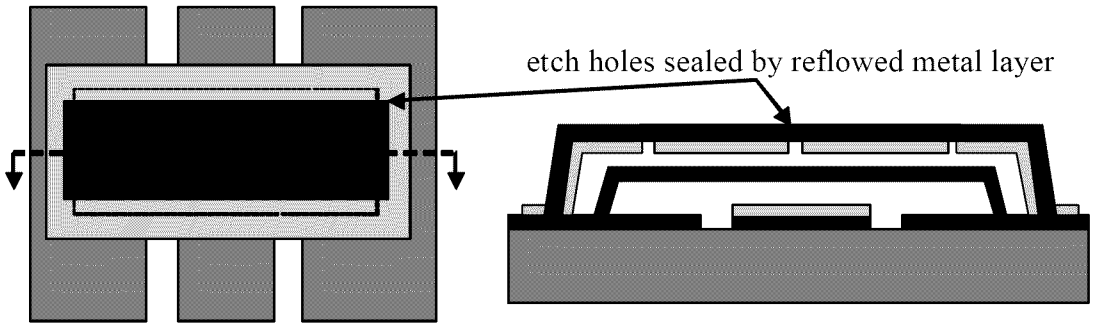


Figure 8.7. (a) Top view and (b) side cut-away drawings of the switch and encapsulation after the final step of the encapsulation fabrication process where the metal layer is reflowed to seal the etch holes. The encapsulation is now hermetically (or near-hermetically) sealed.

8.3. Discussion of Fabrication Process

The proposed process has several advantages. One is that it only requires three masks: the encapsulation sacrificial layer etch mask, the dielectric layer etch mask, and the metal layer lift-off mask. Another advantage is that it uses standard materials and fabrication processes. Another big advantage that is a problem with many packaging technologies is that this is a low-temperature technology. Sputtering is the deposition method used, which is low temperature. By choosing indium as the reflow metal, the maximum temperature the MEMS switch will be subjected to during reflow (~160°C) is well below the given temperature threshold of the MEMS switch of 300-350° C [1].

Although the process has several advantages, some challenges or disadvantages of this process exist. One is that a very high-precision mask alignment is necessary for the etch holes in the metal layer to align with the etch holes in the dielectric layer. This may be alleviated somewhat by using larger holes for the metal layer than for the dielectric layer. For example, some room for error would be given if the etch holes in the dielectric layer are 2 μm and the etch holes in the metal layer are 4 μm. As described in Chapter 7, the size of the etch holes in the metal layer could easily be made larger as long as the thickness of the layer is large enough for the holes to close when the metal is reflowed. Another challenge that may make fabrication difficult is the high aspect ratio required for fabricating the metal layer with etch holes. In particular, a 7-10 μm thick layer of photo-resist must be patterned with feature sizes of 3 μm for the etch holes in the metal layer. It is not clear if this process can be used with high reliability without testing it.

Some issues in the solder reflow step will need to be resolved through further research. For example, it may be possible that a surface cleaning or a flux is necessary in order for the indium solder to reflow freely. Stark and Najafi have demonstrated low temperature fluxless solder reflow for MEMS packaging, but their process employs a solder paste that is defluxed and outgassed prior to applying it to the MEMS device wafer and reflowing it [3]. If a flux gas is used during the reflow step, it will effectively be sealed in the encapsulation. The effects on a MEMS switch's performance and lifetime in the presence of a flux gas is unknown. It may be necessary to use a different low-melting-temperature solder alloy if indium is found to oxidize too rapidly for this method.

Another potential issue in the solder reflow step is the possibility that the solder will not adhere to the silicon nitride layer when reflowed.It may be possible that a metal

adhesion layer is necessary between the indium layer and the silicon nitride layer to ensure proper adhesion of the metal layer to the dielectric layer. According to Kovacs, adhesion layers of reactive metals such as Ti or Cr are often necessary to bond non-reactive metals to other non-metallic materials [4].

8.4. Summary

In this chapter the optimum design for a thin film encapsulation with a metal layer was presented, along with a fabrication process that can be used to manufacture the encapsulation. The optimum design is relatively simple to fabricate using standard thin film techniques, and only includes one post-processing step. The next chapter summarizes the work that was done as part of this thesis and gives recommendations for future areas of work in this area.

8.5. References

[1] Ebel, J. L., personal communications, Dec. 2003.

[2] Source: WebElements [http://www.webelements.com/].

[3] Stark, B. H. and K. Najafi, "A mold and transfer technique for lead-free fluxless solder application to wafer-level low-temperature thin-film packages," in *17th IEEE International Conference on Micro Electro Mechanical Systems, MEMS 2004*, pp. 13-16.

[4] Kovacs, G. T. A., *Micromachined Transducers Sourcebook*, New York, NY: McGraw-Hill, 1998.

9. Conclusions

This chapter summarizes the work that was completed in this thesis, discusses challenges and lessons learned from the process, summarizes the contributions this work made to the MEMS field, and recommends areas for follow on research.

9.1. Summary of Work Completed

This thesis involved several different areas of research all related to the design of high-performance thin film encapsulations for RF MEMS switches. First, the state of the art in RF MEMS packaging was surveyed. Next, encapsulation designs were created based on AFRL RF MEMS switches and dielectric encapsulations. These designs were assessed using equivalent circuit analytical models and full-wave electromagnetic simulation, and were compared to existing test data for the dielectric encapsulated switches. Based on these results, an optimized encapsulation design was proposed, and a novel fabrication process was created to fabricate the encapsulations. In addition, RF feedthroughs were designed and analyzed, and modeling of the metal layer reflow over the etch holes was performed to determine necessary dimensions to guarantee hole closure.

9.2. Challenges Encountered in this Research

The main challenge encountered in this work was the breadth of topics that had to be covered. This work required knowledge in electromagnetics, RF circuits, MEMS fabrication and packaging, and solder reflow. Due to minimal knowledge in many of these areas, much time was spent learning or re-learning the basics. In addition, much of the research involved the use of Ansoft High Frequency Structure Simulator (HFSS), which is a very powerful and capable software tool. It is easy to use right away, but it takes quite a while to learn how to use *well*, where one can have good confidence in the output.

Another challenge was that many of the issues tackled for this thesis have not been considered before, to the best of the author's knowledge. The work could not continue where someone else left off; it had to be started from scratch in many cases. This resulted in a lot of time being spent defining the problem and scoping it down to a manageable research project.

9.3. Lessons Learned

For a project such as this, it would really pay off to set high goals, and start the actual work as early as possible. Yes, adequate time must be given to the literature survey, but the real knowledge comes from the new work that is done. It is important to get some results early, even if they are preliminary or "back-of-the-envelope." Once some results are in hand, they open doors to other more interesting scenarios that can be explored. It is actually a process of refining what the problem is, or what you want it to be, based on what looks most interesting to explore. After the problem has been clearly defined, it can be explored thoroughly. The result is not necessarily *more* work that is completed, but work that is more significant.

9.4. Contributions Made to the MEMS Field

Several novel ideas were proposed and analyzed in this thesis. This is the first research to propose and analyze RF MEMS encapsulations consisting of metal and dielectric that are fabricated with thin film techniques. This research showed that it is feasible to fabricate thin-film encapsulations over RF MEMS switches that have minimal performance degradation on the device, and an optimized encapsulation was designed based on analysis results. Second, this is the first research to consider sealing etch holes by reflowing solder over them as the last step in the encapsulation process. Finally, this is the

first research to model solder reflow over an etch hole in order to determine the necessary dimensions of the etch hole width and metal layer thickness to guarantee the hole will close when the metal is reflowed. These metal reflow contributions will be useful in areas other than RF MEMS packaging.

9.5. Recommendations for Future Work

This research has several logical areas where future work can be done to further the concept of thin film encapsulation with a reflowed metal layer.

9.5.1. Solder Reflow Testing

Several questions have to be answered concerning the reflow of the solder over the etch holes. Some simple laboratory testing on test structures could answer several questions, such as:

- What flux or surface preparation is necessary for reflow?
- Will the indium solder seal the etch holes when reflown?
- Will the indium solder flow onto other areas of the design, where it is not wanted?
- Will the indium solder adhere to the silicon nitride, or are adhesion layers of Ti or Cr necessary below the indium layer?
- What is the rate of flow of the solder when heated?

9.5.2. RF Feed-Through Design

Much work could be done on designing optimized RF feed-throughs into the encapsulation. Ideally, the feed-throughs would make the designs with the "conformal" metal layer feasible. If they were feasible, the fabrication of the switches could be simplified by using the metal layer as the etch mask for the dielectric layer. This would negate the need for a very accurate mask alignment that is required in the proposed process (to

make sure the etch holes in the metal layer align with the etch holes in the dielectric layer).

9.5.3. Fabricate and Test the Encapsulations

The most logical extension of the current work is to fabricate the proposed design. Better yet, fabricate several of the designs to have more data to compare the accuracy of the analytical models and HFSS simulations. Also, the feasibility of the fabrication process would be determined. By fabricating and testing the proposed encapsulations with the proposed fabrication process, the work would likely translate into at least one publishable journal or conference paper, and contribute significantly to the MEMS field.

9.5.4. Improve the Analytical Models

The models in this work were developed independently from the testing and simulation data. If the encapsulations were fabricated and tested, the data could be used in concert with the simulated data to adjust the analytical models to be very accurate. This would involve tweaking the model parameters to match the test and simulation data. With more accurate models, engineers could design encapsulations based on their needs for performance, size, etc.

9.5.5. Analyze Mechanical Strength and Electromagnetic Shielding

An investigation could be carried out on the mechanical strength and electromagnetic shielding contributed to the encapsulation by a metal layer on top. An engineering trade-off probably exists between the metal layer width and the strength and shielding. These trade-offs could be optimized, or put into models for engineers to use to design encapsulations based on their needs.

9.5.6. Analyze Hermeticity of Encapsulations

Metal bonding rings are frequently used to create hermetic seals in flip-chip packaging methods. Hermeticity is a requirement for MEMS switch packaging, so an investigation could be taken on to determine what the hermeticity is of the encapsulations with metal layers.

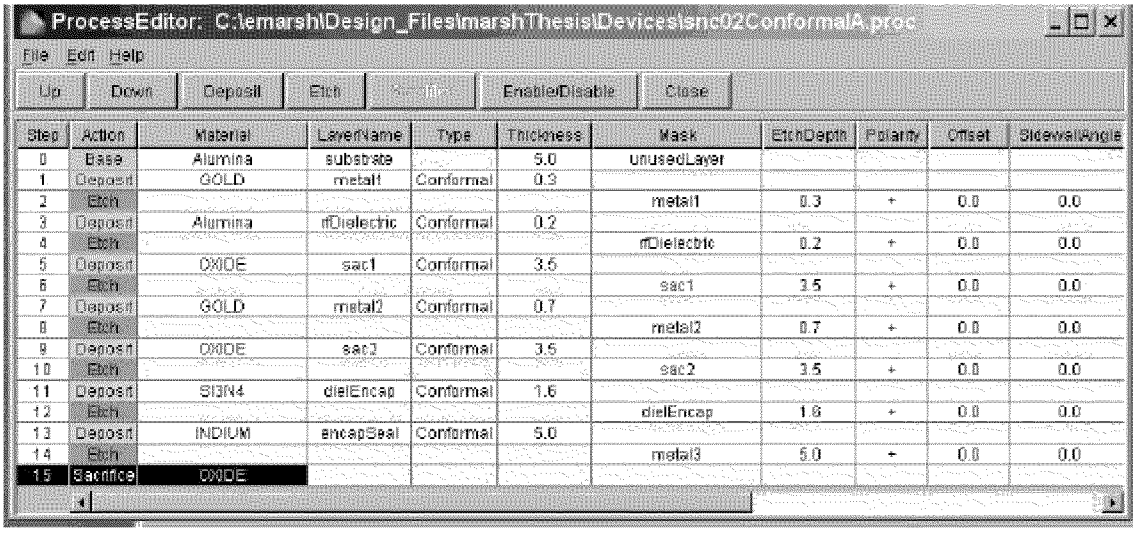
9.5.7. Analyze Reliability of Encapsulated Switches

One of the major goals of packaging is to improve and stabilize device reliability. Does the process or do the materials contribute to poor reliability of the encapsulated switches? How do switch lifetimes of encapsulated switches compare with the unencapsulated switches? Does the solder outgas contaminants into the encapsulation that reduce the lifetime of the switch?

9.6. Conclusion

The research done as part of this thesis successfully designed thin film encapsulations and a fabrication process to manufacture these encapsulations. The performance effects on switch performance due to the encapsulations were assessed, and optimized designs were produced based on the results. The work also included the proposal of a novel solder reflow step to seal the etch holes as the final step of fabrication. This work leads to several areas of follow-on research, namely fabrication and testing of the proposed designs and process. If successful, these proposals could lead to a simple, cost-effective zero-level packaging process, which is one of the current technologies lacking for RF MEMS switches.

Appendix A. Coventorware Settings



Step	Action	Material	LayerName	Type	Thickness	Mask	EtchDepth	Polarity	Offset	SidewallAngle
0	Base	Alumina	substrate		5.0	unusedLayer				
1	Deposit	GOLD	metal1	Conformal	0.3					
2	Etch					metal1	0.3	+	0.0	0.0
3	Deposit	Alumina	rfDielectric	Conformal	0.2					
4	Etch					rfDielectric	0.2	+	0.0	0.0
5	Deposit	OXIDE	sac1	Conformal	3.5					
6	Etch					sac1	3.5	+	0.0	0.0
7	Deposit	GOLD	metal2	Conformal	0.7					
8	Etch					metal2	0.7	+	0.0	0.0
9	Deposit	OXIDE	sac2	Conformal	3.5					
10	Etch					sac2	3.5	+	0.0	0.0
11	Deposit	SI3N4	dielEncap	Conformal	1.6					
12	Etch					dielEncap	1.6	+	0.0	0.0
13	Deposit	INDIUM	encapSeal	Conformal	5.0					
14	Etch					metal3	5.0	+	0.0	0.0
15	Sacrifice	OXIDE								

Figure A.1. Screen capture image from Coventorware showing the details of the fabrication process used to create a solid model from the 2D layout files.

Table A.1. Set-up and analysis settings used in Coventorware for finding the capacitance between the CPW signal line and the MEMS bridge.

Setting	Value
MESH SETTINGS	--
Mesh type	Surface
Element type	3-node triangle
Global element size	10 μm
Boundary refinement level	0
ANALYSIS SETTINGS	--
Analysis Tool	MemCap
Execution Mode	Interactive
Grid Density	0
GridDepth	0
MaxIterations	150
MemcapMemory	InCore
Preconditioner	On
Integration order	2
Number of direct layers	2
Iteration Tolerance	1.0e-4
Stop ratio	0.9
FFT domain scale	1.5
ToolName	MemcapfftTool
SolveOption	Capacitance_Only
CoordType	Original
UseMechLinks	No
RelativePerm	1.000

Appendix B. Capacitance Calculation Computer Code

```
% capacitanceCalcs14Dec.m
% Eric Marsh
% This program calculates the parallel plate capacitance and total capactance
% of RF MEMS switches with and without metal encapsulations. The total
% capacitance is calculated from the parallel plate capacitance by adjusting
% the value for fringing field capacitance and surface roughness.

close all; clear all;
% Input geometries and material parameters for the 18 switch and encapsulation
% configurations.
wCPW = 80e-6;               % Width of signal line of CPW, [m]
wBeam = 120e-6;             % Width of switch beam, [m]
epsilon0 = 8.8542e-12;      % Permittivity of free space
epsilonR1 = 9.2;            % Relative permittivity of rf dielectric
epsilonR2 = 7.0;            % Relative permittivity of encap dielectric
metEncapThick = 5.0e-6;     % Thickness of metal layer of encapsulation, , [m]
bridgeThick = 0.7e-6;       % Thickness of switch beam, [m]
rfDielThick = 0.2e-6;       % Thickness of RF dielectric, [m]
bridgeHeight = [1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 ].*3.5e-6;  % [m]

encapThick = ones(1,18)*1.6e-6;     % Thickness of dielectric encap layer, [m]
encapThick(11:12) = 3.2e-6;

encapHeight = ones(1,18)*3.5e-6;    % Thickness of sacrificial layer that
encapHeight(13:14) = 5.0e-6;        % defines the encapsulation, [m]
encapHeight(17:18) = 6.5e-6;

conformWidth = 200+(2*metEncapThick/1e-6);% Total width of conformal designs,[m]
metEncapWidth = [0; 0; 0; 0;             % Width of metal encapsulation,[m]
    160; 160; 200; 200;
    conformWidth; conformWidth; conformWidth; conformWidth;
    200; 200; 180; 180;
    200; 200]'.*1e-6;

% Calculate parallel plate capacitances in three parts:
%   C1: between signal line and bridge
%   C2: between signal line and upper part of metal encapsulation
%   C3: between signal line and lower part of metal encapsulation (conformed)

c1PP = wCPW*wBeam.*epsilon0./(bridgeHeight+(rfDielThick./epsilonR1));
encapOverlapWidth = (metEncapWidth-120e-6);
encapOverlapWidth(find(encapOverlapWidth>200e-6))=200e-6;
encapOverlapWidth(find(encapOverlapWidth<0))=0;
c2PP = encapOverlapWidth.*wCPW.*epsilon0./((bridgeHeight+bridgeThick+encapHeight)...
    + encapThick./epsilonR2);
c3PP = ones(1,18)*(conformWidth-200)*1e-6*wCPW*epsilon0*epsilonR1./encapThick;
c3PP(find(metEncapWidth<=200e-6))=0;
cTotPP = c1PP+c2PP+c3PP;
cTotPPFf = cTotPP./1e-15;

% Additional capacitance on switch beam and encap due to fringing field capacitance
% Assume no fringing field contribution for switch in down state
c1FF = c1PP.*[   1; 0; 1; 0; 1; 0; 1; 0; 1;
              0; 1; 0; 1; 0; 1; 0; 1; 0]'.*1.458;
c2FF = c2PP.*1.20;
% Reduction in the parallel plate cap.
% due to surface roughness (SR) of the rf dielectric layer
c1SR = c1PP.*[   0; 1; 0; 1; 0; 1; 0; 1; 0;
              1; 0; 1; 0; 1; 0; 1; 0; 1]'.*0.60;
% Total capacitance is the sum of all capacitances because they are in parallel
cTot = c1FF+c2FF+c1SR+c3PP;  %[F]
cTotFf = cTot./1e-15;  %[F]
```

Appendix C. Coplanar Waveguide (CPW) Design Calculations and Computer Code

In designing or analyzing a CPW, it is necessary to calculate its characteristic impedance (Z_0) and its relative dielectric constant (ε_{eff}). The theory described here is from the CPW text by Simons [1]. Consider the CPW shown in Figure C.1. In the figure, a CPW is shown on top of a substrate of finite thickness (h_1). The CPW signal line has a width S and the gap between the signal line and the ground lines is denoted with W. The ground plane traces and the substrate are assumed to be infinite in width. The structure is assumed to be immersed in free space, so the relative dielectric constant outside of the structure is 1.0. The thickness of the CPW conductors is not considered. The first step in finding e_{eff} and Z_0 is to find the capacitance C_{air} between the signal and ground lines in the air space between them:

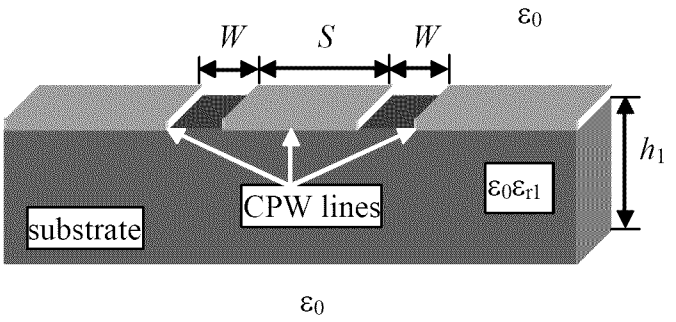


Figure C.1. Drawing of a CPW on a substrate of finite thickness. The ground planes of the CPW and the substrate are assumed to be infinite in width.

$$C_{air} = 4\varepsilon_0 \frac{K(k_0)}{K(k_0')} \tag{C.1}$$

where ε_0 is the permittivity of free space and the arguments of the complete elliptic integrals $K(k_0)$ and $K(k_0')$ are

$$k_0 = \frac{S}{S+2W} \tag{C.2}$$

$$k_0' = \sqrt{1-k_0^2} \tag{C.3}$$

The next step is to calculate the capacitance C_1 in the dielectric substrate:

$$C_1 = 2\varepsilon_0(\varepsilon_{r1}-1)\frac{K(k_1)}{K(k_1')} \tag{C.4}$$

where ε_{r1} is the relative dielectric constant in the substrate, and the arguments of the complete elliptic integrals $K(k_1)$ and $K(k_1')$ are given with

$$k_1 = \frac{\sinh(\pi S/4h_1)}{\sinh\{[\pi(S+2W)]/4h_1\}} \tag{C.5}$$

$$k_1' = \sqrt{1-k_1^2} \tag{C.6}$$

The total capacitance for the CPW C_{CPW} is the sum of the other two capacitances,

$$C_{CPW} = C_{air} + C_1 = 4\varepsilon_0\frac{K(k_0)}{K(k_0')} + 2\varepsilon_0(\varepsilon_{r1}-1)\frac{K(k_1)}{K(k_1')} \tag{C.7}$$

Finally the effective dielectric constant ε_{eff} and the characteristic impedance can be calculated:

$$\varepsilon_{eff} = \frac{C_{CPW}}{C_{air}} = 1 + \frac{(\varepsilon_{r1}-1)}{2}\frac{K(k_1)}{K(k_1')}\frac{K(k_0')}{K(k_0)} \tag{C.8}$$

$$Z_0 = \frac{1}{cC_{air}\sqrt{\varepsilon_{eff}}} = \frac{30\pi}{\sqrt{\varepsilon_{eff}}}\frac{K(k_0')}{K(k_0)} \tag{C.9}$$

where c is the speed of light in a vacuum. The Matlab code used to perform these calculations, as well as the RF feed-through design calculations, is given below.

```
% cpwFeedThroughCalcs.m
% Eric Marsh
% CPW design calculations and calculations for a RF-feed through
% into a MEMS encapsulation with a metal layer

% CPW design/analysis equations from [Simons, p. 20]
% Conventional CPW on a dielectric substrate of finite thickness
% and infinite ground plane widths
eR1 = 9.4;                  % dielectric constant of substrate
e0 = 8.85419e-12;           % dielectric constant of free space, [F/m]
c = 2.997925e8;             % speed of light in vacuum, [m/s]
h = 432e-6;                 % thickness of substrate, [m]
s = [10:1:100].*1e-6;       % width of signal trace, [m]
w = (80e-6)-(s./2);         % gap between ground and signal traces, [m]

k1 = sinh(pi.*s./(4*h))./(sinh((pi.*(s+2.*w))./(4*h)));
k1Prime = sqrt(1-k1.^2);

k0 = s./(s+2.*w);
k0Prime = sqrt(1-k0.^2);

% Note: Matlab computes elliptic integrals K(m) using ellipke(m),
% where m=k^2, so K(k) is calculated with ellipke(k^2)
c1 = 2*e0*(eR1-1)*(ellipke(k1.^2)./ellipke(k1Prime.^2));    %[F]
cAir = 4*e0*(ellipke(k0.^2)./ellipke(k0Prime.^2));          %[F]
cCpw = c1 + cAir;                                           %[F]

% Calculate effective dielectric constant of CPW
eEff = cCpw./cAir;

% Calculate characteristic impedance of CPW
z0 = 1./(c.*cAir.*sqrt(eEff));          % [ohms]

% Plot effective dielectric constant vs. signal line width
figure;
plot(s,z0);
ylabel('Characteristic Impedance, Z_o, \Omega');
xlabel('Width of Signal Line [m]');
grid on;

% Plot CPW characteristic impedance vs. signal line width
figure;
plot(s,eEff);
ylabel('Effective Dielectric Constant, \epsilon_e_f_f');
xlabel('Width of Signal Line [m]');
grid on;

%%%% Use results from above to design a RF feed-through based on
% impedance matching principles
% Input geometry of air bridge and material parameters
e0 = 8.85419e-12;          % Permittivity of free space, [F/m]
c=3e8;                     % Speed of light in vacuum, [m/s]
tDiel=3.2e-6;              % thickness of dielectric layer, [m]
eR2 = 7.0;                 % relative permittivity of dielectric
z0 = 50;                   % characteristic impedance of CPW line, [ohms]
wAB = 5e-6;                % width of air bridge, [m]
```

```
% input impedance and width of high impedance section of t-line,
% calculated from plots above
zH = 70;                    % characteristic impedance of narrow section, [ohms]
wZH = 44e-6;                % width of signal line of modified CPW, [m]
eEff = 5.17;                % effective dielectric constant of modified CPW

% Use theory in [Weller et al, p1637] to calculate the required
% length of high impedance line needed to impedance match the
% air bridge
cAB = wZH*wAB*e0*eR2/tDiel;             % capacitance at air bridge, [F]
L2 = c*zH*z0^2*cAB/(sqrt(eEff)*(zH^2-z0^2));   % intermediate variable
LH = L2-0.7*wAB             % length of modified CPW section, [m]

% For use in analytical model, find equivalent inductance of the
% step change in the CPW center conductor
% theory is from [RF MEMS, Rebeiz]
LStep = zH*(L2B/2)*sqrt(eEff)/c         % inductance of step, [H]
```

C.1 References

[1] Simons, R. N., *Coplanar Waveguide Circuits, Components, and Systems*, New York: Wiley-Interscience, 2001.

Appendix D. Surface Evolver Code

```
// holeUm.fe
// Evolver data for hole in volume of fluid.
// This simulates an etch hole that is patterned in
// solid solder, then reflowed.
// All units are in meters
// Eric Marsh

PARAMETER height = 5.17e-6
// critical ratio (h/w) => 5.170(5.175)/5.0 = 1.034-1.035

vertices
1     0.0          0.0          0.0          fixed
2     45e-6        0.0          0.0          fixed
3     45e-6        45e-6        0.0          fixed
4     0.0          45e-6        0.0          fixed
5     0.0          0.0          height       fixed
6     45e-6        0.0          height       fixed
7     45e-6        45e-6        height       fixed
8      0.0         45e-6        height       fixed
9     20e-6        20e-6        0            fixed
10    25e-6        20e-6        0            fixed
11    25e-6        25e-6        0            fixed
12    20e-6        25e-6        0            fixed
13    20e-6        20e-6        height
14    25e-6        20e-6        height
15     25e-6       25e-6        height
16     20e-6       25e-6        height

edges  /* given by endpoints and attribute */
1     1 2  fixed
2     2 3  fixed
3     3 4  fixed
4     4 1  fixed
5     5 6  fixed
6     6 7  fixed
7     7 8  fixed
8     8 5  fixed
9     1 5  fixed
10    2 6  fixed
11    3 7  fixed
12    4 8  fixed
13    9 10 fixed
14    10 11fixed
15    11 12 fixed
16    12 9  fixed
17    1 9
18    2 10
19    3 11
20    4 12
21    13 14
22    14 15
23    15 16
24    16 13
```

```
25     9 13
26     10 14
27     11 15
28     12 16
29     5 13
30     6 14
31     7 15
32     8 16

faces  /* given by oriented edge loop */
1      1 10 -5  -9  fixed
2      2 11 -6 -10  fixed
3      3 12 -7 -11  fixed
4      4  9 -8 -12  fixed
5      21 -26 -13 25
6      26 22 -27 -14
7      27 23 -28 -15
8      28 24 -25 -16
9      -1 17 13 -18 fixed
10     18 14 -19 -2 fixed
11     19 15 -20 -3 fixed
12     20 16 -17 -4 fixed
13     5 30 -21 -29
14     6 31 -22 -30
15     32 -23 -31 7
16     8 29 -24 -32

bodies  /* one body, defined by its oriented faces */
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16  volume 2000e-12*height
```

Appendix E. Data Comparison and Presentation Computer Code

```
% plotAllDataTHESIS.m
%  Eric Marsh
% This program plots for comparison s-parameter data from testing, analytical
% modeling, and HFSS simulation of RF MEMS switches with and without
% encapsulations made of dielectric and metal
% Creates only the plots that are used in the thesis
%
% Key:  Variable Name Format is 'XYZ', where
%       'X' is the type of data: f=frequency vector, S=s-parameter matrix
%       'Y' is the solution type: A=analytical model; T=test/experiment;
%                                 H=HFSS simulation data
%       'Z' is the RF MEMS switch/encapsulation configuration:
%           1=no encap, up position;
%           2=#1, down position
%           3=dielectric encap, up position
%           4=#3, down position
%           5=dielectric and metal (w=160) encap , up position
%           6=#5, down position
%           7=dielectric and metal (w=200) encap, up position, metal on top
%           8=#7, down position
%           9=dielectric and metal (w=200+) encap, up pos, metal conforms down sides
%           10=#9, down position
%           11=dielectric and metal (w=200+) encap, up, diel thickness 2x
%           12=#11, down position
%           13=dielectric and metal (w=200) encap, sac layer t=5.0
%           14=#13, down position
%           15=dielectric and metal (w=180), up position
%           16=#15, down position
%           17=dielectric and metal (w=200) encap, sac layer t=6.5, up pos.
%           18=#17, down position
close all; clear all;

%%%%%%%%%%%%%%%% Load all Data %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%  1: No Encapsulation, Switch in Up Position %%%%%%%%%%%%%%%%
% Test Data (T1)
% Read in test data from Excel spreadsheet (This reads in test data for all cases)
[ST,header] = xlsread('encapSwitchTestData');
fT=ST(:,1);
ST1 = ST(:,3);

% Analytical Model data (A1)
[SA,header] = xlsread('modelData16Dec');
fA = SA(:,1);
SA1S21 = SA(:,3);
SA1S11 = SA(:,2);

% HFSS Data (H1)
switchUpSParmsE8Dec;
fH1E=f;
SH1E = S;
clear S Z f;

%%%%%%%%%%%%%%%%  2: No Encapsulation, Switch in Down Position %%%%%%%%%%%%%%%%%%
% Test Data (T2)
ST2 = ST(:,7);

% Analytical Model Data (A2)
SA2S21 = SA(:,5);

%HFSS data (H2)
switchDnNoEncapA8Dec;
fH2A=f;
SH2A = S;
clear S Z f;

%%%%%%%%%  3:  Dielectric Encapsulation, Switch in Up Position  %%%%%%%%%%%%%%%%%
```

```
% Test Data (T3)
ST3 = ST(:,5);

% Analytical Model data (A3)
SA3S21 = SA(:,7);
SA3S11 = SA(:,6);

% HFSS Data (H3)
switchUpDielEncapD9Dec;
fH3D=f;
SH3D = S;
clear S Z f;

%%%%%%%%%  4:  Dielectric Encapsulation, Switch in Down Position %%%%%%%%%%%%%%%%
% Test Data (T4)
ST4 = ST(:,9);

% Analytical Model data (A4)  - Same as scenario (2), no encap in down pos.
SA4S21 = SA(:,9);

% HFSS Data (H4)
switchDnDielEncapB9Dec;
fH4B=f;
SH4B = S;
clear S Z f;

%%%%  5:  Dielectric/Metal (w=160) Encapsulation, Switch in Up Position  %%%%%%%%
% Analytical Model Data (A5)
SA5S21 = SA(:,11);
SA5S11 = SA(:,10);

% HFSS Data (H5)
switchUpMet160E9Dec;
fH5E=f;
SH5E = S;
clear S Z f;

%%%%  6:  Dielectric/Metal (w=160) Encapsulation, Switch in Down Position  %%%%%%
% Analytical Model Data (A6)
SA6S21 = SA(:,13);

% HFSS Data (H6)
switchDnMet160B10Dec;
fH6B=f;
SH6B = S;
clear S Z f;

%%%%  7:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%%%%
%%%%      Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
% Analytical Model Data (A7)
SA7S21 = SA(:,15);
SA7S11 = SA(:,14);

% HFSS Data (H7)
switchUpMet200AF16Dec;
fH7F=f;
SH7F = S;
clear S Z f;

%%%%  8:  Dielectric/Metal (w=200) Encapsulation, Switch in Down Position  %%%%%%
%%%%      Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
% Analytical Model Data (A8)
SA8S21 = SA(:,17);

% HFSS Data (H8)
switchDnMet200AB9Dec;
fH8B=f;
SH8B = S;
clear S Z f;
```

```
%%%%  9:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%%
%%%%      Metal Layer Conforms Down Sides of Encapsulation               %%%%%%%%
% Analytical Model Data (A9)
SA9S21 = SA(:,19);
SA9S11 = SA(:,18);

% HFSS Data (H9)
switchUpMet200BA11Dec;
fH9A=f;
SH9A = S;
clear S Z f;

%%%%  10:  Dielectric/Metal (w=200) Encapsulation, Switch in Down Position  %%%%%%
%%%%      Metal Layer Conforms Down Sides of Encapsulation              %%%%%%%%
%% Analytical Model Data (A10)
SA10S21 = SA(:,21);

% HFSS Data (H10)
switchDnMet200BA18Dec;
fH10A=f;
SH10A = S;
clear S Z f;

%%%%  11:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%%
%%%%      Metal Layer Conforms Down Sides of Encapsulation              %%%%%%%%
%%%%      Dielectric Layer Thickness is Doubled to 3.2 um               %%%%%%%%
% Analytical Model Data (A11)
SA11S21 = SA(:,23);
SA11S11 = SA(:,22);

% HFSS Data (H11)
switchUpMet200CA11Dec;
fH11A=f;
SH11A = S;
clear S Z f;

%%%%  12:  Dielectric/Metal (w=200) Encapsulation, Switch in Down Position  %%%%%%
%%%%      Metal Layer Conforms Down Sides of Encapsulation                %%%%%%%
%%%%      Dielectric Layer Thickness is Doubled to 3.2 um               %%%%%%%%
% Analytical Model Data (A12)
SA12S21 = SA(:,25);

% HFSS Data (H12)
switchDnMet200CA18Dec;
fH12A=f;
SH12A = S;
clear S Z f;

%%%%  13:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%%
%%%%       Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
%%%%      Encapsulation Sacrificial Layer is Increased to 5.0 um         %%%%%%%%
% Analytical Model Data (A13)
SA13S21 = SA(:,27);
SA13S11 = SA(:,26);

% HFSS Data (H13)
switchUpMet200DA12Dec;
fH13A=f;
SH13A = S;
clear S Z f;

%%%%  14:  Dielectric/Metal (w=200) Encapsulation, Switch in Down Position  %%%%%%
%%%%      Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
%%%%      Encapsulation Sacrificial Layer is Increased to 5.0 um         %%%%%%%%
% Analytical Model Data (A14)
SA14S21 = SA(:,29);

% HFSS Data (H14)
```

```
switchDnMet200DA14Dec;
fH14A=f;
SH14A = S;
clear S Z f;

%%%%  15:  Dielectric/Metal (w=180) Encapsulation, Switch in Up Position  %%%%%%
% Analytical Model Data (A15)
SA15S21 = SA(:,31);
SA15S11 = SA(:,30);

% HFSS Data (H15)
switchUpMet180A12Dec;
fH15A=f;
SH15A = S;
clear S Z f;

%%%%  16:  Dielectric/Metal (w=180) Encapsulation, Switch in Down Position  %%%%%%
% Analytical Model Data (A16)
SA16S21 = SA(:,33);

% HFSS Data (H16)
switchDnMet180A14Dec;
fH16A=f;
SH16A = S;
clear S Z f;

%%%%  17:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%
%%%%      Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
%%%%      Encapsulation Sacrificial Layer is Increased to 6.5 um         %%%%%%%
% Analytical Model Data (A17)
SA17S21 = SA(:,35);
SA17S11 = SA(:,34);

% HFSS Data (H17)
switchUpMet200EA15Dec;
fH17A=f;
SH17A = S;
clear S Z f;

%%%%  18:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%
%%%%      Metal Layer is Entirely on Top of Encapsulation               %%%%%%%%
%%%%      Encapsulation Sacrificial Layer is Increased to 6.5 um         %%%%%%%
% Analytical Model Data (A18)
SA18S21 = SA(:,37);

% HFSS Data (H18)
switchDnMet200EA15Dec;
fH18A=f;
SH18A = S;
clear S Z f;

%%%%  19:  Dielectric/Metal (w=200) Encapsulation, Switch in Up Position  %%%%%
%%%%      Metal Layer conforms down sides of encapsulation              %%%%%%%%
%%%%      RF feed-through design is assessed                           %%%%%%%
% Analytical Model Data (A19)
SA19S21 = SA(:,39);
SA19S11 = SA(:,38);

% HFSS Data (H19)
switchUpMet200FA14Jan;
fH19A = f;
SH19A = S;
clear S Z f;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%                                                  %%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%   Comparison Plots for Thesis                     %%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%                                                  %%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%%% All Analytical Results - S21 in Up position
figure;
plot(fA,SA1S21,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
%plot(fA,SA3S21,'ks-');
plot(fA,SA5S21,'kv-');
plot(fA,SA7S21,'ko-');
plot(fA,SA9S21,'k*-');
plot(fA,SA11S21,'kp-');
plot(fA,SA13S21,'k.-');
plot(fA,SA15S21,'kx-');
plot(fA,SA17S21,'k^-');
axis tight;
h=legend('no encapsulation',... %'dielectric-only encap',
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
    't_d=1.6, g_e=6.5, w_m=200',3);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
ylabel('\midS_2_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

%%% All Analytical Results - S11 in Up position
figure;
plot(fA,SA1S11,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
%plot(fA,SA3S11,'ks-');
plot(fA,SA5S11,'kv-');
plot(fA,SA7S11,'ko-');
plot(fA,SA9S11,'k*-');
plot(fA,SA11S11,'kp-');
plot(fA,SA13S11,'k.-');
plot(fA,SA15S11,'kx-');
plot(fA,SA17S11,'k^-');
axis tight;
h=legend('no encapsulation',...  %'dielectric-only encap',
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
    't_d=1.6, g_e=6.5, w_m=200',4);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
ylabel('\midS_1_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

%% All Analytical Results - S21 in Down position
figure;
plot(fA,SA2S21,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
%plot(fA,SA4S21,'ks-');
plot(fA,SA6S21,'kv-');
plot(fA,SA8S21,'ko-');
plot(fA,SA10S21,'k*-');
plot(fA,SA12S21,'kp-');
plot(fA,SA14S21,'k.-');
plot(fA,SA16S21,'kx-');
plot(fA,SA18S21,'k^-');
axis tight;
h=legend('no encapsulation',...  %'dielectric-only encap',
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
    't_d=1.6, g_e=6.5, w_m=200',1);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
```

```
ylabel('\midS_2_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

% All HFSS Results - S21 in Up position
figure;
plot(fH1E./1e9,20*log10(abs(SH1E(:,3))),'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH3D./1e9,20*log10(abs(SH3D(:,3))),'ks-');
plot(fH5E./1e9,20*log10(abs(SH5E(:,3))),'kv-');
plot(fH7F./1e9,20*log10(abs(SH7F(:,3))),'ko-');
plot(fH9A./1e9,20*log10(abs(SH9A(:,3))),'k*-');
plot(fH11A./1e9,20*log10(abs(SH11A(:,3))),'kp-');
plot(fH13A./1e9,20*log10(abs(SH13A(:,3))),'k.-');
plot(fH15A./1e9,20*log10(abs(SH15A(:,3))),'kx-');
plot(fH17A./1e9,20*log10(abs(SH17A(:,3))),'k^-');
axis tight;
h=legend('no encapsulation','dielectric-only encap',...
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
    't_d=1.6, g_e=6.5, w_m=200',3);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
ylabel('\midS_2_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

% All HFSS Results - S11 in up position
figure;
plot(fH1E./1e9,20*log10(abs(SH1E(:,1))),'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH3D./1e9,20*log10(abs(SH3D(:,1))),'ks-');
plot(fH5E./1e9,20*log10(abs(SH5E(:,1))),'kv-');
plot(fH7F./1e9,20*log10(abs(SH7F(:,1))),'ko-');
plot(fH9A./1e9,20*log10(abs(SH9A(:,1))),'k*-');
plot(fH11A./1e9,20*log10(abs(SH11A(:,1))),'kp-');
plot(fH13A./1e9,20*log10(abs(SH13A(:,1))),'k.-');
plot(fH15A./1e9,20*log10(abs(SH15A(:,1))),'kx-');
plot(fH17A./1e9,20*log10(abs(SH17A(:,1))),'k^-');
axis tight;
h=legend('no encapsulation','dielectric-only encap',...
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
    't_d=1.6, g_e=6.5, w_m=200',4);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
ylabel('\midS_1_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

%%% All HFSS results - S21, switch in down position
figure;
plot(fH2A./1e9,20*log10(abs(SH2A(:,3))),'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH4B./1e9,20*log10(abs(SH4B(:,3))),'ks-');
plot(fH6B./1e9,20*log10(abs(SH6B(:,3))),'kv-');
plot(fH8B./1e9,20*log10(abs(SH8B(:,3))),'ko-');
plot(fH10A./1e9,20*log10(abs(SH10A(:,3))),'k*-');
plot(fH12A./1e9,20*log10(abs(SH12A(:,3))),'kp-');
plot(fH14A./1e9,20*log10(abs(SH14A(:,3))),'k.-');
plot(fH16A./1e9,20*log10(abs(SH16A(:,3))),'kx-');
plot(fH18A./1e9,20*log10(abs(SH18A(:,3))),'k^-');
axis tight;
h=legend('no encapsulation','dielectric-only encap',...
    't_d=1.6, g_e=3.5, w_m=160','t_d=1.6, g_e=3.5, w_m=200',...
    't_d=1.6, g _e=3.5, w_m=214','t_d=3.2, g_e=3.5, w_m=214',...
    't_d=1.6, g_e=5.0, w_m=200','t_d=1.6, g_e=3.5, w_m=180',...
```

```
    't_d=1.6, g_e=6.5, w_m=200',1);
set(h,'FontName','Times','FontSize',18);
xlabel('Frequency (GHz)','FontName','Times','FontSize',18);
ylabel('\midS_2_1\mid (dB)','FontName','Times','FontSize',18);
set(gca,'FontName','Times');

% Test data, HFSS data, and Model data - S21 in up position
figure;
plot(fT,ST(:,3),'kd-');
hold on;grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fA,SA1S21,'ks-');
plot(fH1E./1e9,20*log10(abs(SH1E(:,3))),'kv-');
plot(fT,ST(:,5),'ko-');
plot(fA,SA3S21,'k*-');
plot(fH3D./1e9,20*log10(abs(SH3D(:,3))),'kp-');
axis([0 26 -0.2 0.01]);
h=legend('test: no encap','model: no encap','HFSS: no encap',...
    'test: dielectric encap','model: dielectric encap',...
    'HFSS: dielectric encap',3);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

% Test data, HFSS data, and Model data - S11 in up position
figure;
plot(fT,ST(:,18),'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18)
plot(fA,SA1S11,'ks-');
plot(fH1E./1e9,20*log10(abs(SH1E(:,1))),'kv-');
plot(fT,ST(:,19),'ko-');
plot(fA,SA3S11,'k*-');
plot(fH3D./1e9,20*log10(abs(SH3D(:,1))),'kp-');
axis tight;
xlim([0 26]);
h=legend('test: no encap','model: no encap','HFSS: no encap',...
    'test: dielectric encap','model: dielectric encap',...
    'HFSS: Dielelctric encap',4);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_1_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

% Test data, HFSS data, and Model data - S21 in down position
figure;
plot(fT,ST(:,7),'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fA,SA2S21,'ks-');
plot(fH2A./1e9,20*log10(abs(SH2A(:,3))),'kv-');
plot(fT,ST(:,9),'ko-');
plot(fA,SA4S21,'k*-');
plot(fH4B./1e9,20*log10(abs(SH4B(:,3))),'kp-');
axis([0 26 -30 0]);
h=legend('test: no encap','model: no encap','HFSS: no encap',...
    'test: dielectric encap','model: dielectric encap',...
    'HFSS: Dielelctric encap',1);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

% Vary metal width: HFSS and model - S21 in Up position
figure;
plot(fA,SA5S21,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
```

```
plot(fH5E./1e9,20*log10(abs(SH5E(:,3))),'ks-');
plot(fA,SA15S21,'kv-');
plot(fH15A./1e9,20*log10(abs(SH15A(:,3))),'ko-');
plot(fA,SA7S21,'k*-');
plot(fH7F./1e9,20*log10(abs(SH7F(:,3))),'kp-');
axis tight;
h=legend('model: w_m=160','HFSS: w_m=160',...
    'model: w_m=180','HFSS: w_m=180',...
    'model: w_m=200','HFSS: w_m=200',3);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

%%% vary the encap sac layer thickness: HFSS and model,
% S21 in up position
figure;
plot(fA,SA7S21,'ks-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH7F./1e9,20*log10(abs(SH7F(:,3))),'kd-');
plot(fA,SA13S21,'ko-');
plot(fH13A./1e9,20*log10(abs(SH13A(:,3))),'kv-');
plot(fA,SA17S21,'kp-');
plot(fH17A./1e9,20*log10(abs(SH17A(:,3))),'k*-');
axis tight;
h=legend('model: g_e=3.5','HFSS: g_e=3.5',...
    'model: g_e=5.0','HFSS: g_e=5.0',...
    'model: g_e=6.5','HFSS: g_e=6.5',3);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

%% vary dielectric thickness - HFSS and model - S21 in up position
figure;
plot(fA,SA9S21,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH9A./1e9,20*log10(abs(SH9A(:,3))),'ks-');
plot(fA,SA11S21,'kv-');
plot(fH11A./1e9,20*log10(abs(SH11A(:,3))),'ko-');
axis tight;
h=legend('model: t_d=1.6','HFSS: t_d=1.6',...
    'model: t_d=3.2','HFSS: t_d=3.2',3);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');

% %% Show RF feed-through results - S11, HFSS and model
figure;
plot(fA,SA11S11,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH11A./1e9,20*log10(abs(SH11A(:,1))),'ks-');
plot(fA,SA19S11,'kv-');
plot(fH19A./1e9,20*log10(abs(SH19A(:,1))),'ko-');
axis tight;
h=legend('model: standard feed-through',...
    'HFSS: standard feed-through',...
    'model: modified feed-through',...
    'HFSS: modified feed-through',4);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_1_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');
```

```
%% Show RF feed-through results - S21, HFSS and model
figure;
plot(fA,SA11S21,'kd-');
hold on; grid on;
set(gca,'GridLineStyle',':','FontSize',18);
plot(fH11A./1e9,20*log10(abs(SH11A(:,3))),'ks-');
plot(fA,SA19S21,'kv-');
plot(fH19A./1e9,20*log10(abs(SH19A(:,3))),'ko-');
axis tight;
h=legend('model: standard feed-through',...
    'HFSS: standard feed-through',...
    'model: modified feed-through',...
    'HFSS: modified feed-through',3);
set(h,'fontname','times');
xlabel('Frequency (GHz)','Fontsize',18,'fontname','times');
ylabel('\midS_2_1\mid (dB)','Fontsize',18,'fontname','times');
set(gca,'fontname','times');
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13. SUPPLEMENTARY NOTES

14. ABSTRACT

Microelectromechanical systems (MEMS) radio frequency (RF) switches have been shown to have excellent electrical performance over a wide range of frequencies. However, cost-effective packaging techniques for MEMS switches do not currently exist. This thesis involves the design of RF-optimized encapsulations consisting of dielectric and metal layers, and the creation of a novel thin film encapsulation process to fabricate the encapsulations. The RF performance of several encapsulation designs are evaluated with an analytical model, full wave electromagnetic simulation, and laboratory testing. Performance degradation due to parasitic and reflection losses due to the package is considered, and RF feed-throughs of the transmission line into and out of the package are designed and assessed.

Ten different encapsulation designs were created and their RF performance was characterized in terms of insertion loss, return loss, and isolation. A switch without an encapsulation and a switch with a dielectric encapsulation were fabricated and tested by the Air Force Research Laboratory (AFRL), and the test data was used to verify the data from analytical modeling and electromagnetic simulation performed in this work. All results were used to design an optimized encapsulation. An RF MEMS switch with this encapsulation was shown to have an overall insertion loss of less than -0.15 dB at 20 GHz compared to an unencapsulated switch insertion loss of about -0.1 dB. The isolation of the switch was slightly improved with the encapsulation.

The fabrication process proposed to manufacture these encapsulations uses a low temperature solder as the metal encapsulation layer. As the final step in the fabrication, the solder is brought to melting temperature and reflowed over the etch holes to form a hermetic encapsulation. Analysis was performed to determine the necessary dimensions of the solder thickness and the etch hole width in order to guarantee that the hole will close when the solder is reflowed. The results found that for a square etch hole with a width of 5 μm, the minimum solder layer thickness to guarantee hole closure is 5.17 μm.

15. SUBJECT TERMS
microelectromechanical systems, electric switches, radiofrequency, microwave frequency, packaging, encapsulation, mathematical models, digital simulation, insertion loss

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